

## **Impact of capacity loss factors in front-of-line IC packaging on production performance: a case study**

**Lee Hsuen Yen**

School of Mechanical Engineering, Universiti Sains Malaysia  
Engineering Campus, 14300 Nibong Tebal, Pulau Pinang, Malaysia  
[hsuenyen@yahoo.com](mailto:hsuenyen@yahoo.com)

**Shahrul Kamaruddin**

Mechanical Engineering Department, Universiti Teknologi PETRONAS, Bandar Seri Iskandar,  
36210, Perak, Malaysia  
[shahrul.k@utp.edu.my](mailto:shahrul.k@utp.edu.my)

**Zulhilmi Paiz Ismadi**

School of Engineering, Monash University Malaysia, Jalan Lagoon Selatan, 47500 Bandar  
Sunway, Selangor Darul Ehsan, Malaysia  
[mohd.zulhilmi@monash.edu](mailto:mohd.zulhilmi@monash.edu)

**Joshua Prakash**

Faculty of Engineering and Green Technology, Universiti Tunku Abdul Rahman, Perak Campus,  
Jalan Universiti, Bandar Barat, 31900,  
Kampar, Perak  
[joshuaj@utar.edu.my](mailto:joshuaj@utar.edu.my)

**Nik Mizamzul Mehat**

Faculty of Engineering Technology, Universiti Malaysia Perlis (UNIMAP), Aras 1, Blok S2,  
Kampus UniCITI Alam, Sungai Chuchuh, Padang Besar 02100, Perlis, Malaysia  
[nikmizamzul@unimap.edu.my](mailto:nikmizamzul@unimap.edu.my)

### **Abstract**

Attributed to the rapidly maturing and evolving application of electronics packaging, efficient packaging processes are crucial in ensuring high quality and reliability of products. One of the elements in efficient packaging processes is the minimization of capacity losses. Most of the devices are patterned onto wafers, specifically for the front of line integrated circuit (IC) packaging. In this area, various capacity loss factors need to be correctly identified and integrated into production planning to prevent low fill rate, expansion of lead time and work-in process (WIP) build-up. This research is based on a case study; wherein potential capacity loss factors of a chosen front-of-line production are investigated to identify their impact on production performance. Mathematical models of various factors are integrated into the simulation model of the current production. The performance measure data are then collected and analysed, thus determining the significant capacity loss factors. It was found that cycle time, setup time, yield loss and machine downtime are significant capacity loss factors in front section of line packaging.

### **Keywords**

Capacity loss, front-of-line packaging, cycle time, yield loss, machine downtime

## 1. Introduction

The inclusion of capacity loss factors in capacity planning is crucial to ensure that an organization maintains profitability. Specifically, for Integrated Circuit (IC) packaging, wherein the demand largely exceeds the facility's capability, failure to address various capacity loss factors can result in low fill rate, hence revenue reduction. Broadly, IC packaging consists of four distinct stages: wafer fabrication, wafer test, IC assembly, and IC test. The former two stages are known as the front of line packaging. In this section, most of the devices are patterned onto the wafer. On the other hand, the latter two stages can be classified as the back-end packaging, where the individual semiconductors are assembled into IC's. Figure 1 depicts the processes that encompass the front of line packaging, as the primary focus of this study.

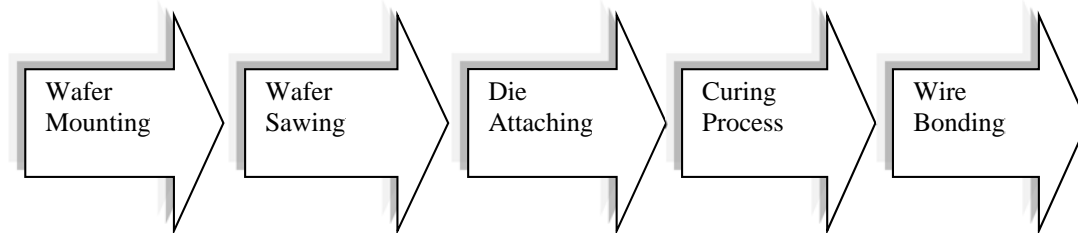


Figure 1: Simplified IC packaging front of line processes

Capacity loss factors are highly specific to industry and facility of application. Nevertheless, the literature reveals that there are several common outlooks on the capacity loss factors and performance measures. For example, Van Roijen et al. (2013) found that cycle time can become a significant capacity loss factor, attributed to various lead counts packages, test times, and number of test steps in the optical gate. Chien and Zheng (2012) explained that both yield loss and process reliability are significant capacity loss factors, attributed to complex package design with nonconforming process parameters. Makani-Lim and Lim (2012) concluded that machine downtime is a crucial capacity loss factor due to the unprecedented expansion of flow time coupled with a reduction in throughput. Kim et al. (2008) and Bard et al. (2012) proved that setup can be a critical capacity loss factor if the setup time is not in equilibrium with the setup frequency. Zhou and Rose (2012) and Chien et al. (2012) stated that WIP level is a capacity loss factor because it affects the utilized capacity. Additionally, Li et al. (2005) concluded that key performance measures for capacity loss evaluation in the semiconductor industry are throughput, machine utilization, flow time and WIP level. This research work investigates the significant capacity loss factors on the performance of a case study front of line processes in Factory A. This paper is organized as follow: section 2 delineates the steps to investigate the significant capacity loss factors. Section 3 describes the design of experiment and the simulation model construction. Results and discussions are presented in Section 5. Section 6 concludes the paper.

## 2. Methodology

The methodology consists of five sequential stages, and is explained below:

### *Step 1: Determine potential capacity loss factors*

The potential capacity loss factors are cycle time, yield loss, machine downtime, machine setup and WIP level. The inherent characteristics of the capacity loss factors are based on an empirical study. The factors are influenced by each other and difficult to be isolated without adversely affecting another factors.

### *Step 2: Develop mathematical models*

Heuristic equations of each factor are formulated to be integrated into the simulation model. Changes in the variable values will determine the significance of the capacity loss factors in the performance measure.

#### *a) Cycle time model*

The operation cycle time,  $T_c$ , is defined as the time taken for the completion of one unit of part. The equation, highlighted by Groover (2008), can be expressed as

$$T_c = T_o + T_h + T_t, \quad (1)$$

where  $T_c$  = operation cycle time (min/pc),  $T_o$  = time of the actual processing operation (min/pc),  $T_h$  = handling time (min/pc) and  $T_t$  = tool handling time (min/pc).

b) *Yield model*

The Poisson model assumes the defect distribution is random and sequence-independent (Kim and Oh, 2006). Let  $Do$  = average of defects per unit area and  $A$  = device area,  $\lambda$  = average defects on particular chip, the probability that a chip contain  $k$  defect is

$$P(k) = \frac{\lambda^k e^{-\lambda}}{k!} = \frac{(ADo)^k e^{-ADo}}{k!}, \quad (2)$$

where  $\lambda = ADo$ ,  $k = 0, 1, 2, \dots$

Since manufacturing yield is defined by the probabilistic of a chip that contain zero defects, therefore, yield is mathematically denoted as

$$Y_{poisson} = P(0) = e^{-\lambda} = e^{-ADo} \quad (3)$$

The negative binomial model is used when the defect density (clustering) is random, as shown in a study by Guikema and Goffelt (2008). The negative binomial yield model is given by

$$Y_{NB} = P(0) = \frac{1}{(1 + \frac{ADo}{\alpha})^\alpha} = (1 + \frac{ADo}{\alpha})^{-\alpha} \quad (4)$$

where  $\alpha$  = cluster factor.

c) *Machine downtime model*

Machines downtime is often related to the machine availability, which is a common measure of reliability for equipment. A quick approximation of the availability of a system under ideal conditions is given by the formula

$$A = \frac{MTBF}{MTBF + MTTR} \quad (5)$$

where  $A$  = availability,  $MTBF$  = mean time between failures (hr) and  $MTTR$  = mean time to repair (hr) (Gholami et al., 2009).

d) *Setup model*

We assume a setup time,  $S_{ij}$ , is required if a job  $j$  follows job  $i$ . All the jobs are assumed available at  $t=0$ . Consider the job sequence  $Q = \{i(0), i(1), \dots, i(k(Q))\}$  and  $(J-Q)$  is the set of remaining tasks. The task  $\Psi\{i[k(Q)]\}$  which will succeed  $i\{k(Q)\}$  can only be started after a minimal time of setup after the completion time of  $i\{k(Q)\}$ . The minimal setup time

can be expressed by following formula as shown by Souissi et al., (2004),

$$S_{min}\{i[k(Q)]\} = \min_{j \in (J-Q)} \{S_{i[k(Q)],j}\} \quad (6)$$

e) *WIP Model*

The WIP level in the system is determined by subtracting a target WIP level in the system from the current WIP level in the system. The equation can be shown as below (Disney and Towill, 2003):

$$Total\ WIP = \max(0, \sum_{j=0}^{n_p} W_p^j - \sum_{j=0}^{n_p} w_p^j), \quad (7)$$

where  $n_p$  = number of workstation for product  $p$ ,  $W_p^j$  = target WIP level at the  $j$ -th workstation of product  $p$  and

$w_p^j$  = current WIP level at the  $j$ -th workstation of product  $p$ .

*Step 3: Design of experiment (DOE)*

Single case (factor) experiment design is used to determine the significance of the capacity loss factors. The experiment consists of two major groups, namely control and treatment groups. Control group refers to the model that is derived with the current condition of the factory, whereas treatment group consists of four subgroups that relates to the reduction of factors. The subgroups are the reduction of 5%, 10%, 20% and 30% of each factor. Five replications using different pseudo-random number streams drive the simulation.

*Step 4: Build simulation model*

Simulation has become a popular technique for developing production schedules and dispatching lists in a manufacturing environment. In this paper, the simulation model is developed using WITNESS2007. It is build according to the work flow diagram as illustrated in Figure 2.



Figure 2: Front of line work flow diagram

There are seven workstations in the model including wafer mount, wafer saw, second optical, die attach, epoxy cure oven, wire bond and third optical. Several assumptions made are: a) raw materials are 100% available, b) manning ratio is optimized, and c) each part input represent one unit of product. Each machine is subjected to a cycle time and setup time. Wire bond machine includes downtime and repair specified by an Erlang distribution. A warm-up period of twenty-four hours is used. The model is set to run 220 lots and will be stopped after the 220 lots are completed. Model verification is done via visual checking to identify correct flow of parts. Model validation is conducted by comparing performance measures with historical data.

*Performance measures used in experiments*

Three performance measures used are average flow time, throughput rate and make span.

a) *Average Flow Time*

Average flow time can be defined as the time taken to produce one completed product. It is expressed as:

$$\text{Average flow time} = \text{Sum of flow time for all units} / \text{Numbers of units completed} \tag{10}$$

b) *Throughput rate*

Throughput rate is the average number of products completed in a unit of time. It can be expressed as:

$$\text{Throughput rate} = \text{Number of products completed} / \text{Completion time} \tag{11}$$

*c) Make Span*

Make span is defined as the different between of the completion time of last operation and starting time of the first operation. The equation is expressed as:

$$\text{Make Span} = \text{Completion time of last operation} - \text{starting time of first operation.} \quad (12)$$

*Step 5: Analysis of results using ANOVA*

ANOVA is used to uncover the main and interaction effects. One-way ANOVA is carried out and followed by Dunnett test to compare the treatment groups with the control group.

### 3. Simulation Results

*Experiment 1: Analysis of cycle time*

From Table 1,  $F_{\text{test}}$  of all performance measures are larger than  $F_{\text{crit}}$ . Therefore, all null hypotheses are rejected and the effect of cycle time on average flow time, throughput rate and make span is significant.

Table 1. Summarized table for ANOVA on Experiment 1

| Performance Measures | $F_{\text{test}}$ | Inference   | Level of Significance |
|----------------------|-------------------|-------------|-----------------------|
| Average flow time    | 247.37            | Significant | 0.01                  |
| Throughput rate      | 278.04            | Significant | 0.01                  |
| Make span            | 510.44            | Significant | 0.01                  |

$$F_{\text{crit } 0.99}(4,20) = 4.43 \text{ and } F_{\text{crit } 0.95}(4,20) = 2.87$$

From the Dunnett Test in Table 2, the treatment condition, T, for all groups exceed  $T_{\text{stat}}$ . This shows that the reduction of cycle time in the group means for all performances is significant.

Table 2. Summarized table for Dunnett Test on Experiment 1

| Performance Measures | Treatment condition, T         | Inference | Level of Significance |           |
|----------------------|--------------------------------|-----------|-----------------------|-----------|
| Average Flow Time    | Reduction of 5% on cycle time  | 4.6136    | Significant           | 0.01      |
|                      | Reduction of 10% on cycle time | 8.9054    | Significant           | 0.01      |
|                      | Reduction of 20% on cycle time | 18.0791   | Significant           | 0.01      |
|                      | Reduction of 30% on cycle time | 27.8026   | Significant           | 0.01      |
| Throughput Rate      | Reduction of 5% on cycle time  | 3.5840    | Significant           | 0.01 0.01 |
|                      | Reduction of 10% on cycle time | 7.2407    | Significant           | 0.01      |
|                      | Reduction of 20% on cycle time | 16.5371   | Significant           |           |
|                      | Reduction of 30% on cycle time | 29.3265   | Significant           | 0.01      |
| Make Span            | Reduction of 5% on cycle time  | 5.6457    | Significant           | 0.01 0.01 |
|                      | Reduction of 10% on cycle time | 12.7649   | Significant           | 0.01      |
|                      | Reduction of 20% on cycle time | 24.6729   | Significant           |           |
|                      | Reduction of 30% on cycle time | 39.9548   | Significant           | 0.01      |

$$T_{\text{stat } 0.99}(4,20) = 3.08 \text{ and } T_{\text{stat } 0.95}(4,20) = 2.30$$

*Experiment 2: Analysis of yield loss*

In Table 3,  $F_{test}$  of make span are is larger than  $F_{crit}$ , while  $F_{test}$  of average flow time and throughput rate does not exceed  $F_{crit}$ . The null hypothesis of the yield loss on average flow time and throughput rate experiments is accepted while the null hypothesis of yield loss factors on make span is rejected.

Table 3. Summarized table for ANOVA on Experiment 2

| Performance Measures | $F_{test}$ | Inference     | Level of Significance |
|----------------------|------------|---------------|-----------------------|
| Average flow time    | 0.95       | Insignificant | -                     |
| Throughput rate      | 0.97       | Insignificant | -                     |
| Make span            | 6.73       | Significant   | 0.01                  |

$$F_{crit 0.99}(4,20) = 4.43 \text{ and } F_{crit 0.95}(4,20) = 2.87$$

In Table 4, the treatment condition, T, for each of groups in make span do not exceed  $T_{stat}$ . The reduction of yield loss on the groups means for make span is insignificant.

Table 4. Summarized table for Dunnett Test on Experiment 2

| Performance Measures | Treatment condition, T         | Inference | Level of Significance |
|----------------------|--------------------------------|-----------|-----------------------|
| Make Span            | Reduction of 5% on yield loss  | 2.1513    | Insignificant         |
|                      | Reduction of 10% on yield loss | 1.5049    | Insignificant         |
|                      | Reduction of 20% on yield loss | 1.5049    | Insignificant         |
|                      | Reduction of 30% on yield loss | 2.1513    | Insignificant         |

$$T_{stat 0.99}(4,20) = 3.08 \text{ and } T_{stat 0.95}(4,20) = 2.30$$

*Experiment 3: Analysis of machine downtime*

In Table 5,  $F_{test}$  of average flow time and make span are larger than  $F_{crit}$  for 99% confidence interval, while  $F_{test}$  of throughput rate is larger than  $F_{crit}$  for 95% confidence interval. Each of the null hypotheses is being rejected and the effect of machine downtime on all performance measures is significance, for 95% confidence interval.

Table 5. Summarized table for ANOVA on Experiment 3

| Performance Measures | $F_{test}$ | Inference   | Level of Significance |
|----------------------|------------|-------------|-----------------------|
| Average flow time    | 6.95       | Significant | 0.01                  |
| Throughput rate      | 3.28       | Significant | 0.05                  |
| Make span            | 8.40       | Significant | 0.01                  |

$$F_{crit 0.99}(4,20) = 4.43 \text{ and } F_{crit 0.95}(4,20) = 2.87$$

The Dunnett Test in Table 6 shows T for 30% reduction of machine downtime in average flow time, throughput rate and make span exceed  $T_{stat}$  at 0.01 level of significance. The 20% reductions of machine downtime is significant for average flow time and make span, while the 5% and 10% reduction groups are not significant as T do not exceed  $T_{stat}$ . This shows that only the 20% and 30% reduction groups in machine downtime produce significant effect.

Table 6. Summarized table for Dunnett Test on Experiment 3

| <b>Performance Measures</b> | <b>Treatment condition, T</b>        |        | <b>Conclusion</b> | <b>Level of Significance</b> |
|-----------------------------|--------------------------------------|--------|-------------------|------------------------------|
| Average Flow Time           | Reduction of 5% on machine downtime  | 0.3838 | Insignificant     | -                            |
|                             | Reduction of 10% on machine downtime | 0.7879 | Insignificant     | -                            |
|                             | Reduction of 20% on machine downtime | 3.3130 | Significant       | 0.01                         |
|                             | Reduction of 30% on machine downtime | 3.5756 | Significant       | 0.01                         |
| Throughput Rate             | Reduction of 5% on machine downtime  | 0.1360 | Insignificant     | -                            |
|                             | Reduction of 10% on machine downtime | 1.2242 | Insignificant     | -                            |
|                             | Reduction of 20% on machine downtime | 1.8136 | Insignificant     | -                            |
|                             | Reduction of 30% on machine downtime | 3.1058 | Significant       | 0.01                         |
| Make Span                   | Reduction of 5% on machine downtime  | 0.0054 | Insignificant     | -                            |
|                             | Reduction of 10% on machine downtime | 0.2251 | Insignificant     | -                            |
|                             | Reduction of 20% on machine downtime | 2.6913 | Significant       | 0.05                         |
|                             | Reduction of 30% on machine downtime | 4.5449 | Significant       | 0.01                         |

$T_{stat\ 0.99}(4,20) = 3.08$  and  $T_{stat\ 0.95}(4,20) = 2.30$

*Experiment 4: Analysis of setup time*

Table 7 indicates that  $F_{test}$  of make span is larger than  $F_{crit}$ , while  $F_{test}$  of average flow time and throughput rate do not exceed  $F_{crit}$ . The null hypothesis on make span is being rejected and the alternative hypothesis is accepted. However, the null hypotheses of setup time on average flow time and throughput rate are accepted.

Table 7: Summarized table for test of significant on Experiment 4

| <b>Performance Measures</b> | <b><math>F_{test}</math></b> | <b>Conclusion</b> | <b>Level of Significance</b> |
|-----------------------------|------------------------------|-------------------|------------------------------|
| Average flow time           | 1.29                         | Insignificant     | -                            |
| Throughput rate             | 1.27                         | Insignificant     | -                            |
| Make span                   | 9.49                         | Significant       | 0.01                         |

$F_{crit\ 0.99}(4,20) = 4.43$  and  $F_{crit\ 0.95}(4,20) = 2.87$

Table 8 shows the result of Dunnett Test of the setup time factor on make span. The treatment condition, T for reductions of 30% group in make span exceed  $T_{stat}$  at 0.01 level of significance.

Table 8: Summarized table for Dunnett Test on Experiment 4

| Performance Measures | Treatment condition, T         |        | Conclusion    | Level of Significance |
|----------------------|--------------------------------|--------|---------------|-----------------------|
| Make Span            | Reduction of 5% on setup time  | 0.0542 | Insignificant | -                     |
|                      | Reduction of 10% on setup time | 1.0577 | Insignificant | -                     |
|                      | Reduction of 20% on setup time | 0.4899 | Insignificant | -                     |
|                      | Reduction of 30% on setup time | 4.3759 | Significant   | 0.01                  |

$T_{stat 0.99}(4,20) = 3.08$  and  $T_{stat 0.95}(4,20) = 2.30$

*Experiment 5: Analysis of work-in-progress (WIP) loss factors significancy on the performance measures*

From Table 9, the analysis indicates that three  $F_{test}$  values are less than  $F_{crit}$ . The null hypotheses are accepted for all three performance measures which are no significant effect on average flow time, throughput rate and make span. Thus, no Dunnett Test is carried out since WIP is not a significant loss factor.

Table 9: Summarized table for test of significant on Experiment 5

| Performance Measures | F-Test Value | Conclusion    | Level of Significance |
|----------------------|--------------|---------------|-----------------------|
| Average flow time    | 0.29         | Insignificant | -                     |
| Throughput rate      | 0.26         | Insignificant | -                     |
| Make span            | 0.09         | Insignificant | -                     |

$F_{crit 0.99}(4,20) = 4.43$  and  $F_{crit 0.95}(4,20) = 2.87$

### 3.1 Discussion

Reduction of cycle time is vital to retain capacity yield in the industry. Based on the mathematical model of cycle time (Eqn. (1)), it is proven that the processing cycle time and batch quantity affect the cycle time in progress. Practitioners are advised to reduce the batch quantity in order to diminish the effect of capacity loss. Yield loss in the production line is controlled on 2% in overall production. 2% defect variety is a restricted yield loss limit. Therefore, it can be said that the reduction of yield loss factor only plays a minor role in capacity loss reduction. The yield loss factor only significance on the total production measures, i.e. make span. In the Dunnett Test, only 20% and 30% reduction of machine downtime show significant comparison with the control group. Hence, large reduction on machine downtime can be translated to better production yield. Practitioners can increase the mean time between failures, or reduce the mean time for repair, thus increasing the machine availability and reducing machine downtime. Setup time has limited effect on the average flow time and throughput rate. Despite the situation, setup time influences the total production, such as make span of product in the production line. In the Dunnett Test analysis, only a large percentage of reduction on setup time has significant effect on the performance measures. This occurrence is due to the setup time is less than the operation cycle time. Hence, the small percentage of setup time does not affect the overall productivity of the organization. In the examination of WIP significance, the low  $F_{test}$  value indicates that there is sampling variation in the experiment. In other words, WIP is not a significant capacity loss factor that may lead to productivity constraint in the front of line in IC packaging industry.



#### **4. Conclusion**

This study describes a theoretical method in examining the significant capacity loss factors in the front of line of IC packaging industry. Five major capacity loss factors noted from literature review (cycle time, yield loss, machine downtime, setup time and WIP) have been pinpointed for determining the significance of the factors based on a case study. Five experiments are designed to test on the significance of the loss factors on average flow time, throughput rate and make span. The analysis indicates that cycle time, yield loss, machine downtime and setup time are the significant capacity loss factors in front line of IC packaging industry. The reduction of cycle time and machine downtime greatly affects the performance measures. On the other hand, only larger reduction percentage on yield loss and setup time will influence the factory performance eventually. It has been found that WIP is not significant in the front of line. Future work involves investigation of the capacity loss factors in end of line IC packaging to obtain detailed overview of capacity loss factors and their specific cause throughout the packaging line.

#### **Acknowledgements**

The authors acknowledge the YUTP-FRG grant (0153AA-E36) provided by Yayasan UTP for funding the study that resulted in this article.

#### **References**

- Zisgen, H., Meents, I., Wheeler, B.R. and Hanschke, T., A queueing network based system to model capacity and cycle time for semiconductor fabrication, *Proceedings of the 40th Conference on Winter Simulation*, 07 – 10 December, Miami, Florida, 2008.
- Kim, S., Lee, Y.H., Yang, T. and Park, N. Robust production control policies considering WIP balance and setup time in a semiconductor fabrication line, *The International Journal of Advanced Manufacturing Technology*, vol. 39 no. 3-4, pp. 333-343, 2008.
- Zhou, Z. and Rose, O., WIP balance and due date control in a wafer fab with low and high volume products, *Proceedings of the Winter Simulation Conference*, 09 - 12 December, Berlin, Germany, 2012
- Guikema, S.D. and Goffelt, J.P., A flexible count data regression model for risk analysis. *Risk Analysis*, vol. 28 no. 1, pp. 213-223, 2008.
- Gholami, M., Zandieh, M. and Alem-Tabriz, A., Scheduling hybrid flow shop with sequence-dependent setup times and machines with random breakdowns, *The International Journal of Advanced Manufacturing Technology*, vol 42 no.1-2, pp.189-201, 2009
- Disney, S.M. and Towill, D.R., On the bullwhip and inventory variance produced by an ordering policy, *Omega*, vol. 31 no. 3, pp. 157-167, 2003.
- Van Roijen, R., Conti, S.G., Keyser, R., Arndt, R., Burda, R., Ayala, J. and Yu, C., Reducing environmentally induced defects while maintaining productivity, *IEEE Transactions on Semiconductor Manufacturing*, vol. 26 no. 1, 35-41, 2013.
- Chien, C.F. and Zheng, J.N., Mini-max regret strategy for robust capacity expansion decisions in semiconductor manufacturing, *Journal of Intelligent Manufacturing*, vol. 23 no. 6, pp. 2151-2159, 2012
- Makani-Lim, B. and Lim, F.C., A Set Theory-Based Approach for Efficient Diagnosis of Semiconductor Test Equipment, *Journal of Supply Chain and Operations Management*, vol. 10 no.1, pp. 24, 2012.
- Bard, J.F., Gao, Z., Chacon, R. and Stuber, J., Real-time decision support for assembly and test operations in semiconductor manufacturing, *IIE Transactions*, vol. 44 no. 12, pp. 1083-1099, 2012
- Chien, C.F., Hsu, C.Y. and Hsiao, C.W., Manufacturing intelligence to forecast and reduce semiconductor cycle time, *Journal of Intelligent Manufacturing*, vol. 23 no. 6, pp. 2281-2294, 2012

## **Biographies**

**Lee Hsuen Yen** is an engineer with one of the electronic packaging industry in Penang Malaysia. She obtained her Bachelor Degree in Manufacturing Engineering from Universiti Sains Malaysia.

**Shahrul Kamaruddin** is an Associate Professor at the Mechanical Engineering Department, Universiti Teknologi PETRONAS (UTP), Bandar Seri Iskandar, Perak Darul Ridzuan, Malaysia. He graduated with B.Eng. (Hons) degree from University of Strathclyde, Glasgow, Scotland in 1996, the M.Sc. degree from University of Birmingham, U.K., in 1998, and the PhD from University of Birmingham, in 2003. He also has various past experiences with manufacturing industries from heavy to electronics industries especially in the field of industrial engineering, manufacturing processes and product design. He has more than 200 publications in reputed international, national journals and conferences. He currently served as an Editorial Board member of Cogent Engineering journal.

**Mohd Zulhilmi Paiz Ismadi** is a Lecturer in Mechanical Engineering, Monash University Malaysia, Malaysia. He earned his Bachelor's and Doctoral degree from Monash University, Australia. Throughout his career, he has published several high-impact journal papers and presented in conferences. He is actively involved in industrial projects in various scale from small and medium enterprises to large multinational companies. He is a Chartered Engineer and member of the Institution of Mechanical Engineers, United Kingdom as well as the Institution of Engineers Australia. His research interest involves simulation, image and data processing as well as prediction.

**Joshua Prakash** is an assistant professor at the Department of Industrial Engineering, Faculty of Engineering and Green Technology, Universiti Tunku Abdul Rahman. He obtained his Bachelor Degree in Manufacturing Engineering, and his PhD in Mechanical Engineering, from Universiti Sains Malaysia. He has published papers in international journals. His research area of interest includes manufacturing systems, production planning and control, and lean manufacturing. He also serves as a technical consultant to multiple factories in Malaysia.

**Nik Mizamzul Mehat** received the B.Eng.(Hons) degree from National University of Malaysia, Bangi, Selangor in 2000, the M.Sc. degree from Universiti Sains Malaysia, Nibong Tebal, Penang, in 2010 and PhD in Manufacturing Technology from Universiti Sains Malaysia, Nibong Tebal, Penang, in 2015. She was a trainee engineer at Kolej Kemahiran Tinggi MARA Balik Pulau, Penang, Malaysia and currently is a Senior Lecturer at Department of Mechanical Engineering Technology, Faculty of Engineering Technology, Universiti Malaysia Perlis (UniMAP), Perlis, Malaysia. Her research interests include manufacturing and machining processes, mould manufacturing and plastic processing, plastic flow analysis, process optimization, inter-relationships between processing parameters, mechanical properties and material microstructures related to plastic material and composites. At present, she has published more than 40 publications in reputed international journals/conferences.