Lot Sizing: Optimization of Economic Order Quantity

Herwina Richelle Andres
Operations Research
Analog Devices Philippines
General Trias, Cavite
Philippines
HerwinaRichelle.Andres@analog.com

Abstract

Lot size and set-up frequency are inversely related. Moreover, small lot sizes results to frequent set-ups which reduce the production efficiency. In Company HRA, single small lots are approximately 60% of the total and are scheduled across the weeks. The primary cause of the small test lots is the small lots received into pretest. The current scheduling system is based from actual customer demand which does not take into account the manufacturing efficiency metrics. Therefore, the schedule could contain a requirement of a single die or a number significantly less than the assembled quantity. In this paper, a method was developed for increasing the assembly lot sizes while balancing the test lot size, set-up frequency, cost, and finished goods inventory. The approach was to modify the Economic Order Quantity to take into account the uncertainty inherited in the demand. In addition, parts are classified by their 8 week test volume. Parts that have on average more than 24 hours of demand per week are considered high volume parts and are not bumped up. All others parts are entered into the EOQ formula. The new test lot sizes will be converted into full wafer requirements and larger lots are then scheduled into assembly. This provides HRA the opportunity to schedule larger test lots which will improve the efficiency and reduce the number of set-ups for the same device over multiple weeks. Results show that the set-up per million ratio on the pilot group improved by 24%. In addition, test lots with processing time of greater than 12 hours increased by 19%. These show that the modified EOQ formula best calculates the optimal lot sizes which in turn will yield positive improvement in the company's manufacturing metrics.

Keywords
Lot size, Economic Order Quantity, Set-up frequency, Test schedule

Biography
Herwina Richelle C. Andres received her B.Sc. degree in Industrial Engineering (IE) from Mapua Institute of Technology in 2010. She is currently taking her M.Sc. degree in IE at the University of the Philippines. She is with Analog Devices Inc. Philippines since 2010 as an Operations Research Engineer specializing on manufacturing simulations.