

Microstructural and Electrical properties of Screen-printed N+ Emitter of P-type Monocrystalline Silicon Solar cell

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Abstract

We fabricated the p-type monocrystalline silicon (Si) solar cell with phosphorus (P) screen-printed n+ emitter junction and investigated its microstructural and electrical properties. During P screen-printed n+ emitter process, a 16 nm-thick phosphosilicate glass (PSG) layer was formed as a result of interaction between P-dopant paste and Si substrate. Due to the PSG reflow associated with the reduction of viscosity of oxide caused by the amount of P atoms in PSG layer, thinner and thicker PSG film was formed in convex and concave regions of the textured Si surface, respectively, which was quite different from the growth behavior of thermally grown SiO_2 layer. Due to a strong dependence of P diffusion on the Si interstitials, deeper and shallower junctions were abnormally formed near the convex and concave regions in the textured Si surface, respectively. The electric field and temperature dependence of the current-voltage characteristics demonstrated that the Poole-Frenkel barrier lowering mechanism along with the generation-recombination mechanism had dominance over the current conduction in the reverse bias region of p-type monocrystalline Si solar cell fabricated using screen printing process.

Keywords

Solar cell, Screen Printing, Emitter, PSG, Current Conduction

Biography

Include author bio(s) of 200 words or less.

Chel-Jong Choi is currently an associate professor of Chonbuk National University, Jeonju, Korea. He received the B.S. degree in ceramic engineering from Hanyang University, Seoul, Korea, in 1997, and the M.S. and Ph.D. degrees in materials science engineering from the Gwangju Institute of Science and Technology (GIST), Gwangju, Korea, in 1999 and 2003, respectively. From 2003 to 2005, he was with the Samsung Advanced Institute of Technology (SAIT), Suwon, Korea, in the areas of semiconductor-device characterization. From 2005 to 2008, he worked with the Electronics and Telecommunications Research Institute (ETRI), Daejon, Korea, where he was involved in the process integration of nano-scaled Schottky barrier MOSFETs. Since 2008, he has been with Chonbuk National University, Jeonju, Korea. His research interests include high efficiency solar cells and the novel nanoscaled Ge- and III-V- based electronic devices for the ultimate CMOS and post-CMOS technologies.