Enabling CMOS 0.13µm technology at 0.18µm equipment platform on 200mm Semiconductor Manufacturing Industry

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Abstract—Today’s semiconductor manufacturing industry needs to improve its competitiveness by enabling new technologies and capabilities using existing equipments. Literature show many improvements made in enabling CMOS 0.13µm technology at 0.18µm equipment platform on 200mm. This will avoid the need for additional dedicated equipments, or equipment upgrades. The fabrication process must improve to a level to increase process margin within the product specification. Almost all the capability enhancements need Capital Expenditure (CAPEX). However, enabling new technology through process improvement is the most challenging approach and usually needs very minimum capital expenditure. This paper will discuss real implementation of process improvement that successfully enabled CMOS 0.13µm technology at 0.18µm equipment platform where Shallow Trench Isolation (STI) was a constraint. The approach presented in this paper is through re-design of process development on forming new profile of STI that results in a new physical structure that is able to hold the isolation needed when current flow throughout the chip. This study utilized dataPower yield management system application, wafer position method, inline data collection and process matching. The results were successfully implemented to enable the capability for CMOS 0.13µm technology in existing factory and minimize CAPEX for 200mm semiconductor manufacturing.

Keywords— Process integration; Complementary Metal-oxide Semiconductor (CMOS); Capital Expenditure (CAPEX); Shallow Trench Isolation (STI); Semiconductor fabrication

I. INTRODUCTION

Semiconductor fabrication industry (fabs) is one of the most capital intensive [1] and complicated industries and it is driven by Moore’s Law to continue cost reduction and technology enhancement. In order to sustain semiconductor business, the industry needs to improve its competitiveness by enabling similar equipment platforms to enable more new technology capabilities [2]. Fig. 1 indicated with transforming the main technology node from 0.18µm to 0.13µm and it will result in 45% total die gain per wafer [3]. Traditionally, transforming the main node technology from 0.18µm to 0.13µm, we will need additional dedicated equipment to be purchased, equipment to be upgraded and wafer fabrication process to be improved to the level of increasing process margin within the product specification. Almost all the capability enhancements require CAPEX [1][4]. However, in order to enable new technology through process improvement is the most challenging approach but it results in very minimum CAPEX.

As the device is scaled down from 0.18µm to 0.13µm in 200mm wafer fabs, the equipment platform has offered many new challenges for semiconductor manufacturing. The systematic wafer edge yield loss is one of the major yield loss contribution [2][4][5][6] during initial technology development due to equipment capability and process margin. As 0.13µm technology process integration was reviewed and understood, Shallow Trench Isolation (STI), transistor and backend interconnect directly impact the device’s performances and a detail study is required [7]. The biggest challenge of the 0.13µm STI is to find an operating process window for the edge yield fallout due to High Density Plasma (HDP) deposition void that causes poly stringer after poly deposition process.

STI is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor devices. The STI scheme starts from STI masking on pad nitride, after the dry etch process to form the active island and shallow trench; wet cleaning process is applied to remove the polymer residue. Liner oxidation processes included in this stage to control the STI corner rounding and to fix the damaged induced during the STI plasma dry etch. The trench will be filled with the dielectric material – High Density Plasma (HDP) and planarization by Chemical Mechanical Polishing (CMP) process. Pad nitride will be removed using phosphoric acid to form the STI structure as shown in Fig. 2.
For better isolation process on 0.13µm technology, the isolation aspect ratio scaling has been studied. Fig. 3 illustrates typical aspect ratio scaling from the 0.25µm to 0.07µm technology nodes indicated that the aspect ratio is increased by 66% from 1.589 to 2.643 going from 0.18µm technology to 0.13µm technology in order to maintain the junction capacitance [10]. The aspect ratio scaling for both semiconductor devices spacing is driven by the HDP process gap-fill capability of the process and equipment. During the gap-fill capability evaluation, it is very important to understand the aspect ratio of the minimum design rule. This is determined by the ratio of the sum of the STI trench depth and nitride thickness to the minimum space of design rule critical dimension (CD).

High Density Plasma (HDP) Chemical Vapor Deposition (CVD) deposition is the standard for STI oxide fill of high aspect ratio trenches on 0.18µm and 0.13µm technologies. This was due to its topography compatibility with CMP process and seamless void free for tight trench geometry. Gap-fill improvement strategies using HDP has been discussed by various authors [11][12][13]. Most of the research emphasized on optimization on the deposition and sputter (D/S) ratio [12][13] and aspect ratio for better gap-fill capability. However, little research has been done on the STI special wall structure for the gap-fill mechanism. Therefore, this study is also to understand the interaction impacts between the STI special wall structure, aspect ratio, D/S ratio and HDP-CVD equipment capability on 0.13µm technology.
II. METHODOLOGY

The methodology is defined in Fig. 4 and it divided into 4 parts which is data collection and validation, 0.13µm yield loss characterization, process improvement and new process implementation. This paper will discuss critical findings and approach in the methodology process.

1. Data collection and result validation: Two high runner 0.13µm technology devices, L1 and K8 were selected on this study. In order to make the result are more conclusive, total 1000 low yield wafers per device are used on this study and all the results are validated by wafer sort test. First, it started with data collection of 3000 wafer sort data for device K8 and L1 were retrieved from the dataPower yield management system. Based on the sort yield trend chart, 1000 low yields wafer was identified and it is used on this study. Sample of the raw data show in Table 1.

<table>
<thead>
<tr>
<th>Lot</th>
<th>Sort Yield</th>
<th>Bin8 SIDD Leakage</th>
<th>Bin50 Gamma Test</th>
<th>Bin6 SRAM-BIST</th>
<th>Bin5 Register</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Edge Center Random</td>
<td>Edge Center Random</td>
<td>Edge Center Random</td>
<td>Edge Center Random</td>
</tr>
<tr>
<td>Lot1</td>
<td>80%</td>
<td>10.0%</td>
<td>1.0%</td>
<td>1.2%</td>
<td>0.3%</td>
</tr>
<tr>
<td>Lot2</td>
<td>75%</td>
<td>13.0%</td>
<td>0.2%</td>
<td>0.1%</td>
<td>0.2%</td>
</tr>
<tr>
<td>Lot3</td>
<td>82%</td>
<td>9.0%</td>
<td>0.2%</td>
<td>1.0%</td>
<td>0.1%</td>
</tr>
<tr>
<td>Lot4</td>
<td>78%</td>
<td>11.0%</td>
<td>0.5%</td>
<td>1.0%</td>
<td>0.4%</td>
</tr>
<tr>
<td>Lot5</td>
<td>80%</td>
<td>8.0%</td>
<td>0.2%</td>
<td>0.8%</td>
<td>0.5%</td>
</tr>
<tr>
<td>Lot6</td>
<td>81%</td>
<td>7.0%</td>
<td>0.2%</td>
<td>0.8%</td>
<td>0.3%</td>
</tr>
<tr>
<td>Lot7</td>
<td>79%</td>
<td>9.0%</td>
<td>0.5%</td>
<td>1.0%</td>
<td>0.4%</td>
</tr>
</tbody>
</table>
2. The 0.13µm main yield loss identification: Based on the 1000 low yielding wafers, reorder the failure bins based on decreasing order and analyzed the top three failure bins signature with cumulative wafer sort map. Once the failure signatures were identified, the correlation analysis started with electrical parametric, inline measurement and inline inspection map by wafer levels. This will help to identify any strong correlating parameters to the failure bin. Wafer position tracking analysis is conducted by lot level. This technique was used to identify the affected process steps, tools and down to chamber level based on the lot failure pattern such as bimodal, continuously increasing or decreasing by wafer sequence failure signatures. This technique is capable of wafer position tracking of individual process and equipment throughout entire process that consist of at least 400 process steps on 0.13µm technology. Unique wafer positional histories are recorded for all wafers throughout the entire fabrication process to resolve most of the elusive sources of yield loss and process variation. Equipment commonality and physical failure analysis tabulated to identify the root cause of yield loss. Based on the above description, results shows in Fig. 5.

![Workflow for Low Yield Lot Investigation Techniques](image)

Fig. 5. Workflow for Low Yield Lot Investigation Techniques

3. Process optimization: This stage started with the process mapping and Cause-of-Effect diagram to narrow down the most significant yield loss impact process. Process evaluation and characterization were conducted with Design of Experiment (DOE) methods. Inline defect inspection using KLA-Tencor 2367UV/Visible bright-field inspection system, electrical parametric test and sort test are used to validate each experiments performance as illustrated in Fig. 6.

![Process Optimization Workflow](image)

Fig. 6. Process Optimization Workflow

4. Process implementation: Fig. 7 shows the process implementation workflow. The pre-requisite is for the new optimized process to be verified and meet the requirement with good process margin. Process qualification must be planned to confirm the process, equipment capability and device life testing. For initial phase process implementation, a small volume on one device with new optimized process is released for process stability validation. Inline measurement, electrical parametric and sort test verification are the final condition before fan out to other 0.13µm devices. New optimize process is released after the confirmation of the process capability with good margin on multi devices.

![Process Implementation Workflow](image)

Fig. 7. Process Implementation Workflow
III. RESULT AND DISCUSSION

A. 0.13µm Technology Main Yield Loss Identification

In this research, two 0.13µm high runner production devices with 1000 low yield wafers validated by sort test were selected. The analysis was based on the high major failure bins, failure signatures and cumulative sort map. Fig. 8 showed the failure sort bins Pareto Chart for both devices L1 and K8. Both devices showed wafer edge with high static leakage failure and is the main contribution for the yield loss on 0.13µm technology. A detail sort map correlation analysis to inline inspection was conducted to validate the source of the wafer edge yield loss as shown in Fig. 9. Both sort test map in Fig. 9a and inline defect inspection data map in Fig. 9b are well correlated and the top view SEM images in Fig. 9c. This shows the yield loss were due to deposition void that was detected after pad nitride strip process step. On the top view SEM images, it also observed that the deposition void defect only happens on the special wall structure with specific direction.

In order to validate the failure mechanism, the Scanning Electron Microscope (SEM) physical failure analysis was performed. The cross section SEM, as shown in Fig 10 indicates that the main root causes of the edge leakage failure is due to Poly stringers and the defect was formed due to deposition void. The deposition void happened during the HDP oxide deposition and poly filled into the void during subsequent poly deposition process. This impacted the device leakage and the stringers short between two semiconductor devices. The deposition void that happens in 0.13µm and below technology nodes are mainly due to high aspect ratio requirement with the tight STI spacing and high deposition to physical sputter (D/S) ratio because of the process and equipment hardware capability. Wafer edge observed more deposition void because wafer edge sputtering rate is lower compared to center, resulting in high D/S ratio.

Fig. 8. 0.13µm Technology Main Yield Loss (a) Product K8 and (b) Product L1

Fig. 9. Sort map to inline inspection correlation study (a) Sort Yield Binmap, (b) Inline Inspection Defect Map and (c) Inline SEM Topview
B. Process Characterization and Optimization

Experiments were carried out on 200mm 0.18µm platform Applied Materials Centura Utima HDP-CVD reactors. It consists of two RF coil which allows the independent turning of the plasma in order to achieve a good uniform density across the wafer. The wafer was biased negatively with respect to plasma to provide energy for ion sputtering. Generally, the process chemistries used in HDP-CVD includes SiH$_4$, O$_2$ and diluents such as Ar, He and H$_2$. During deposition process, the wafer was not chucked and backside helium cooling was not implemented.

HDP-CVD gap-fill improvement literature [11] can be categorized into two approaches, which are aspect ratio and deposition to physical sputter (D/S) ratio. In this study, a special STI wall structure tagging approach is included to resolve the deposition void issue.

- Aspect ratio process optimization: The aspect ratio of a STI trench gap is defined by the ratio of the trench height or depth to its width. HDP-CVD oxide gap-fill capability with the deposition and re-deposition process is primarily driven by the aspect ratio, lower the aspect ratio have provided good gap-fill capability. STI spacing split evaluation conducted to understand impact of the gap-fill capability. Based on the experimental result, the deposition void defect has improved by increasing the STI spacing and is in line with previous study [15]. By increasing the STI space, the active island of the semiconductor device is reduced and impacts the semiconductor device performance especially on narrow width semiconductor device, where the active island critical dimension is one of the sensitive parameter to control the semiconductor device performances. Increasing the STI spacing also impacted the island mask printing lithographic process margin on current lithographic ASML® PAS 5500-300C® DUV tool, it caused island mask resist lifting due to smaller active island CD. In order to minimize the impact of the STI lithographic process margin and semiconductor device performance. Low level 3nm of STI space is increased.

- Deposition to physical sputter (D/S) ratio process optimization: HDP-CVD oxide deposition process is through the deposition and sputtering simultaneously. The deposition due to ions and neutrals, contributes to a bottom-up films with very little sidewall growth. The sputtering ion bombardment generated by an RF electrode power. The deposition/sputtering rate ratio (D/S) is an important measure of the gap-filling capability of the processes. The ratio is defined as below

\[
D/S = \frac{(\text{net deposition rate} + \text{blanket sputtering rate})}{\text{blanket sputtering rate}}
\]  

(1)

In general, the use of a lower D/S ratio is for higher aspect ratio structures. Fig. 11 shows high net deposition rate at the wafer edge because of the equipment hardware design is such that SiH$_4$ gasses flows from the wafer edge to center. As a result, the wafer edge deposition rate is high compared to the center region. Fig. 12 shows low sputtering rate at wafer edge. The RF coil that generates RF plasma is located at the center of the chamber. This results high sputtering rate at the center compared to wafer edge. The interaction of the high deposition rate and low sputtering rate at the wafer edge results in the formation of voids.
The deposition void can be addressed by increasing the RF bias power which also increasing directional deposition and re-deposition. In high aspect ratio technology like 0.13µm node, the HDP-CVD deposition is divided into two steps, the first step is a low deposition rate process used for gap-fill and second step used for deposition with high deposition rate. In this study, the focus is on the first step that is used for gap-fill. Table II shows that with increment of the bias RF power to increase the sputtering rate; or reduce the side SiH₄ gasses for reduced the deposition rate provide better gap-fill capability with low deposition void defect. This is aligned with the low D/S ratio have good gap-fill capability. Considering the change of the SiH₄ gas flow will change the oxide films properties, which may affect the device performance. This may result in longer process qualification time; therefore increasing the bias RF power process is a more cost effective solution and was selected. DOE was conducted with different bias RF power to understand the impact of the bias RF power.

The results showed that the deposition void defects were not significant reduced once the bias RF power beyond 300watt. This is because of the deposition and sputtering ratio balancing. From the experimental results, we can conclude that the additional 300watt bias RF power increased the re-deposition process and can improve the gap-fill process margin. This did not fully resolve the deposition void issues.

### TABLE II. SUMMARY OF HDP CVD PROCESS PARAMETERS VS DOI DEFECT ON K8 DEVICE

<table>
<thead>
<tr>
<th>HDP-CVD Process Parameter</th>
<th>Inline Inspection Performance (DOI defect) - count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bias RF (+300Watt)</td>
<td>10</td>
</tr>
<tr>
<td>Bias RF (-300Watt)</td>
<td>&gt; 5000</td>
</tr>
<tr>
<td>O₂ flow (+10sccm)</td>
<td>123</td>
</tr>
<tr>
<td>O₂ flow (-10sccm)</td>
<td>80</td>
</tr>
<tr>
<td>Side SiH₄ (+5sccm)</td>
<td>&gt; 5000</td>
</tr>
<tr>
<td>Side SiH₄ (-5sccm)</td>
<td>200</td>
</tr>
</tbody>
</table>
With the combination approaches of aspect ratio and deposition to sputtering ratio, the sort yield improved by 2.0% as shown in Fig. 14. However, the wafer edge special wall structure deposition void defect still not fully resolved. This was due to the current equipment capability. The next approach is to focus on the special STI structure design optimization.

- STI wall structure design optimization: Deposition void only happens at wafer edge STI wall structure with special direction as shown in Fig. 9c. This study is focus on the custom tagging the weak STI structure with Mentor Graphics' Calibre CAD. Tagging is the function of post Optical Proximity Correction (OPC) that applied to the unique structures with additional pre-defined rules. To prevent the post OPC tagging impact, device performance and integrate process margin, some special rules are defined as below:-
  1. Tagging is only allowed on wall structures that the line end pass the minimum design rule requirement.
  2. Wall structure overlay with Poly is not allowed to do the tagging.
  3. Post OPC tagging required to pass the technology minimum design rule requirement especially contact to island overlap.

Custom post OPC tagging is shown in Fig. 13, the spacing of the special STI wall structures has increased by around 20nm. It has significantly reduced the STI aspect ratio and improved the HDP gap-fill capability. An experiment was carried out to understand the interaction on STI gap-fill capability on new post OPC customs tagging structure Tag2A. Table III summarizes the interaction of engineering split results, the deposition void defect was not fully eliminated but was optimized with STI spacing and HDP-CVD bias RF. With the combination of Tag2A STI new optimized wall structure, the deposition voids defect were fully eliminated with good process margin and overcome the HDP-CVD equipment capability.

![Fig. 13. Special wall structure with custom OPC tagging](image)

### TABLE III. SUMMARY OF ENGINEERING SPLIT ON ISLAND OPC TAGGING, STI SPACING AND HDP-CVD PROCESS CONDITION ON K8 DEVICE

<table>
<thead>
<tr>
<th>STI OPC</th>
<th>STI Spacing</th>
<th>HDP-CVD</th>
<th>Inline Inspection Result (DOI Count)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Old</td>
<td>POR</td>
<td>POR</td>
<td>120</td>
</tr>
<tr>
<td>Old</td>
<td>POR</td>
<td>POR+300W Bias RF</td>
<td>20</td>
</tr>
<tr>
<td>Old</td>
<td>POR-7nm</td>
<td>POR</td>
<td>&gt;5000</td>
</tr>
<tr>
<td>Old</td>
<td>POR-7mm</td>
<td>POR+300W Bias RF</td>
<td>100</td>
</tr>
<tr>
<td>Tag2A</td>
<td>POR</td>
<td>POR</td>
<td>0</td>
</tr>
<tr>
<td>Tag2A</td>
<td>POR</td>
<td>POR+300W Bias RF</td>
<td>0</td>
</tr>
<tr>
<td>Tag2A</td>
<td>POR-7nm</td>
<td>POR</td>
<td>0</td>
</tr>
<tr>
<td>Tag2A</td>
<td>POR-7mm</td>
<td>POR+300W Bias RF</td>
<td>0</td>
</tr>
<tr>
<td>Tag2A</td>
<td>POR-11nm</td>
<td>POR</td>
<td>10</td>
</tr>
<tr>
<td>Tag2A</td>
<td>POR-11nm</td>
<td>POR+300W Bias RF</td>
<td>0</td>
</tr>
</tbody>
</table>

### C. Process Implementation

The new optimized process that consists of Tag2A post OPC tagging on special wall structure, increased 3nm STI spacing with increased 300watt HDP bias RF power process was proven and validated to solve the wafer edge deposition
void defect with good process margin. Process and device qualification with 3 different lots were conducted and it pass the requirements. Small volume 125 wafers were released on one high runner K8 0.13µm device for inline process stability check, inline measurement, inline defect confirmation, electrical parametric and sort test verification. The test result passed all the device specification requirement and sort yield improved by 10% compared to old process. The new optimized process was fanned out to other 0.13µm devices L1 and X5. All inline performances were validated and it passed all the inline and Electrical test specification requirement and free of deposition void defect. 250 wafers sort test that run on new optimize process was validated with yield improving by 10% as shown in Fig. 14.

![0.13µm Sort Yield Improvement with New Optimize Process](image)

**Fig. 14.** Sort Yield performance on Process Of Record (POR) versus New Process.

IV. CONCLUSION

In this study yield optimization for 0.13µm devices processed on 0.18µm equipment platform had been successfully implemented. Wafer edge deposition void at the special STI wall structure was identified as the main contributor for the 0.13µm technology device yield loss. Aspect ratio and deposition to sputter (D/S) ratio that were correlated to the gap-fill capability were studied. Through re-optimization the RF biasing for STI HDP process was increased to increase the re-deposition rate and reduce the wafer edge aspect ratio with increasing the STI spacing. Both processes has improved the gap-fill capability but not fully solved the wafer edge deposition void defect on special wall structure. This new process combined with the post OPC Tag2A tagging on the special wall structure, the results show successful elimination of the wafer edge deposition void defect with good process margin on current 0.18µm HDP-CVD equipment platform. In order to increase the confidence level on the new optimized process, it was implemented on a few higher runner 0.13µm devices. Inline inspection and sort yield validation on 250 wafers confirmed the new optimize process eliminated the wafer edge deposition void issue and sort yield improved by 10%. The results were successfully implemented and able to enable the capability for CMOS 0.13µm technology in existing factory and minimize CAPEX for 200mm semiconductor manufacturing.

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