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Development of Comprehensive WIP Performance Monitoring Systems for Semiconductor Fabrication Foundry

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***Abstract*— Complementary Metal Oxide Semiconductor (CMOS) is a complex and very delicate process in semiconductor. In typical 30,000 wafer capacNity of single foundry business model, the CMOS product loads are mixed from various technologies to serve wider market segments. Total devices can be ranged from 100 to 200. This approach creates variables for process time, equipment usage, number of processing steps which leads to inconsistent WIP profiling at respective time period. A simple indication bar chart to indicate WIP quantity profile at each step is not able to indicate the overall cycle time status of WIP. Literature discussed method needed to apply for WIP planning, but limited for WIP monitoring approaches. This paper is a research regards new approach to develop WIP monitoring parameters that able to show current WIP performance, DPML performance, current WIP to allow strategy to improve WIP planning that resulted for optimize output at effective cycle time. This paper will illustrated the arithmetic for WIP parameter and real case study of approach used from the parameters in the WIP profile data to output and cycle time improvement. The benefits of this information has successfully directed to new WIP strategy that improve the quarterly output by 10% and cycle time at reasonable cycle time.**

Keyword: Day per Mask Layer (DPML), Work In Progress (WIP), WIP profile, CMOS, Foundry

I. INTRODUCTION

Semiconductor manufacturing processes consist of four basic phases: wafer fabrication, wafer probe, assembly, and final testing as shown in Fig. 1. Among all the semiconductor process, wafer fabrication is the most complex requiring and the highest capital investment of semiconductor manufacturing [1]. It requires processing steps from 300 to 1000 and 30 to 90 days cycle time to complete dependent to complexity[2] [2]. In addition to these manufacturing characteristics, the continues demand for shorter cycle time and at 100% on time delivery (OTD) commitment to minimize miss supply chain planning scheduling is a critical means to gain market competitiveness in wafer fabrication industries[3].

The first step to understand the issue is by having the right indices available. In semiconductor data usually kept in the Manufacturing Execution System (MES)[4], [5]. Today almost 100% of the commercial wafer fab using MES and the standards are defined in SEMI [6]. There are many researches in the similar area extracting data from MES for improvement purposes which include metrology sampling to help right WIP are used for measurements at minimum risk while minimizing

the impact of the cycle time [7]. Research in improving MES performance to ensure it can support huge data for reporting were also widely discussed and integrated in commercial software like FactoryWorks, SiView, Promise, 300 Works and many other [8]–[10][11]. However, most commercial software is critical in providing transaction from data based. Customize information required integrating data from MES into open source platform[5] [8], [12]

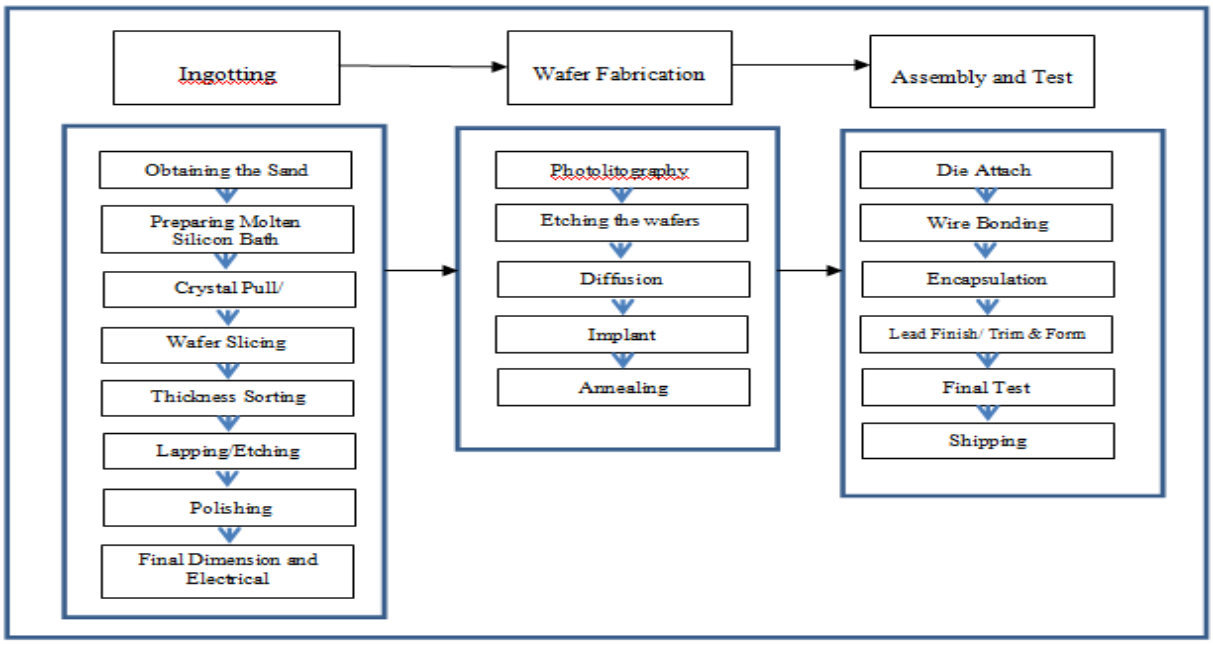


Fig. 1: Semiconductor Flow From Ingotting, Wafer Fabrication and Assembly Test

Wafer fabrication is considered as one of the most complex manufacturing processes because of reentrant processing flow, batch processing, sequence dependent setups, unpredictable tool failure and so on, which differentiate wafer fab from other traditional flow shops or job shops. Dispatching is one of the major techniques to help to smooth manufacturing process, lower inventory level and meet due date[13]. Most of the current dispatching rules are related to due date. They are variants of classical rules like Critical Ratio (CR), Earliest Due Date (EDD) and Operation Due Date (ODD)[14][15][11], [16]. There are also numbers of operational control policies which target the control of inventory level of work center or operation like Minimum Inventory Variability Scheduler (MIVS)[17]. While the first set of dispatching rules do not primarily lead to low inventory level, the later ones do not always lead to good on-time delivery performance. For this reason, some researchers address the complementary strength of WIP balance and due date control.

There are hundreds of wafer products in a wafer fab[18]. Some products are referred to low volume products such as test, sample, small order and new product which have low release rate e.g. dozens of wafers are released per week, while some products are referred to high volume products like common commodity type which has a higher release rate than low volume products. Low volume products are often have a tight target due date and are more critical than high volume products with respect to cycle time and delivery reliability because of due date commitment to the customer [19]. Low volume products are expected to go through the fab as soon as possible, at least meet the target cycle time and due date. However, there is a basic assumption that low volume products suffer from specific machine constraints like higher batch time, longer setup waiting time and less qualified machine available, etc. In addition, local rules change the target function of global rules in order to make a compromise between due date and local constraints. For instance, a WIP balance target between the machines seems to reduce the weight of due date control, because a WIP balance approach would rather push an early lot to an empty machine instead of push a tardy lot to a crowded machine. Therefore, with regard to WIP balance and due date control, there are two main questions for low volume products:
(1) Whether due date is sacrificed by achieving WIP balance;
(2) How to make trade-off if due date is desired more than WIP balance.
These impose an additional challenge to the operational control in a wafer fab.

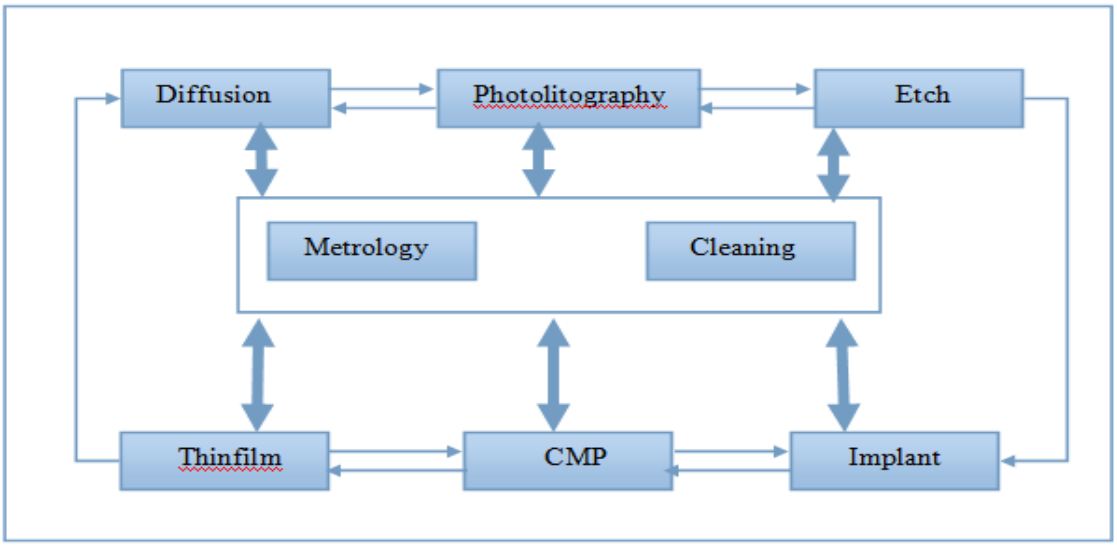


Fig. 2: Typical Wafer Fabrication Process

There are many characteristics of wafer fab like in Fig. 2, such as re-entrance processing flow, batch tools, sequence dependants set up, unpredictable equipment failure and so on, which differentiate wafer fab from other traditional flow shop or job shop. Normally, release strategy and dispatching strategy are two major ways which are applied to control the wafer fab with the purpose of decreasing average cycle time and cycle time variance, achieving on time delivery of the products. Many methods were used on applying the dispatching strategy to wafer fab.
As the process are too complex, automation methods used to improve the productivity and managing the Work In Progress (WIP) materials. There is strong correlation between cycle time and the factory utilization. As the utilization increase, the cycle time may deteriorate. With the WIP increase, the queue time to process will also increase.
Due to the delicate semiconductor process, the high queue time to process will increase respective process especially at higher reentrance level. Cycle time in wafer fabrication is measured by day per mask layer (dpml). It is a method to measure the reentrances at lithography process.

Day Per Mask Layers is an indices in wafer fabrication industry to monitor the cycle time (CT) or Turn Around Time (TAT). It is measuring by the average of the mask layers being processed during the fabrication step. Mask is the circuitry design to print on the wafers during the fabrication process. It has multi layers during the lithography or stepper process.

A. WIP Control

Theory of Constraint said the performance of the factory or FAB is determined by the performance of the bottleneck area. It is necessary to determine an adequate WIP level for the bottleneck to avoid starvation and to support the whole fab to achieve its maximum throughput while running at the minimum WIP level. However, if the WIP level of the bottleneck exceeds the desired WIP level while achieving the maximum throughput of the whole fab, the cycle time is degraded. Lots will spend a significant queue time in front of the bottleneck work center, which will also cause a WIP imbalance to the line. Therefore, a minimum workload is defined for the bottleneck work center. If the actual workload of the bottleneck drops to the minimum workload, the bottleneck is fed with lots to prevent starvation. A maximum workload is also taken into account. If the actual workload of the bottleneck is higher than the maximum workload, bottleneck feeding is stopped to avoid extraordinary queue time, especially, when the bottleneck is broken down.

[7]studied a single dynamic bottleneck in the fab where the bottleneck is the work center with the highest utilization. The minimum and maximum workload for the bottleneck is defined as 12 hours and 24 hours respectively which are defined by the engineers.

Although the bottleneck is the most critical work center which determines the performance of the whole fab, feeding empty non-bottleneck work centers can also smooth the material flow, avoid capacity losses of machines, and improve product cycle times. Therefore, a minimum workload 1.5 hours is also defined for the non-bottleneck work centers. If the workload of

non-bottlenecks drop to this minimum workload level, lots are scheduled to feed it to avoid starvation.

Production Control (PC) will assign the layers output for each process. Production Control main function is to ensure the On Time Delivery (OTD) for each devices and volumes for each Customers are met. Production Control has the privilege to upgrade and downgrade the lots to ensure the OTD are protected. At the same time PC will also has the function to control the WIP movement. PC will apply the Line Balancing concept to maximize the moves and utilization by applying Starvation Avoidance concept to ensure there is no resources are idle. PC function as FAB planners are very critical and important to make sure the resources are busy and moving the right WIP. PC will be responsible for the resources' daily planning move and output.

In typical Integrated Module (IM) activity, PC will assign moves or output for each IM based on the resource capacity and the capability to the IM to produce the moves or the output. Due to the re-entrants process, PC will assign a balancing target moves or output for each layers. The plan is done through manual calculation and it will be uploaded to the system to track the moves and the output. A report to monitor the output hourly will be automated through email and the reporting system to ensure the right layers and moves or output achieved.

The Line Balancing concept is important and by developing the WIP Profile report, it will help the PC and Manufacturing Manager to manage the WIP movement. Since the processes are re-entrants , any spike WIP in the WIP Profile show the real time issue face by the line. It can be due to tools downtime, or WIP congested due to capacity constraint. Applying Bottleneck Management (BN) concept or Theory of Constraint (TOC) is deem needed to ensure the BN resources which determine the FAB capacity are fully loaded with WIP. At the same time it is also important to avoid high WIP waiting at the BN resources. The PC function is important to avoid the WIP pile up and queue in front of the BN resources by moving the WIP to resources that starving or idle.

B. Developing WIP Profile Report

Manufacturing Execution System (MES) mainly used to manage WIP and equipment automation in the FAB. Huge amount of data are recorded automatically in multiple databases during fabrication process where the data become the input to monitor lot movements in the semiconductor fabrication plant, or shortly FAB. MES database composed of a collection of sub systems, each with a specific task contributes to huge database because every single transaction needs to be recorded.

In Fig. 3, the WIP Profile has been designed using the concept of small data warehouse by understanding and analyzing the business needs in this FAB. Based on the current framework and the application layout, the report generator architecture has been constructed using the concept of top down view as shown in Figure 3 above. This approach will select only the relevant information needed for faster data retrieval and accuracy.

The data retrieves mainly from MES application to get the WIP, movement and process flow information[11], [20]. This data will be consolidating with other external application that is APF repository data. In addition, external custom data from the user also will be used for this process. Data from multiple databases will be on cleansing, de-duplication and transformation to more reliable and meaningful data. In this design, we are using a query to summarize the data and it will be store into a data mart. Materialized view concepts also have been used for efficient data retrieval. Materialized views have been found to be very effective in speeding up query as well as update processing[21] A few server have been schedule to run the automated jobs to generate the summarize data. Users are able to view this information through web page, Reporting System or even email.

WIP profile report is developed to manage the line balancing. It is also a way to monitor the WIP movement and will give indicators on how the FAB WIP are staging.
The FAB WIP is divided to 7 sub areas:
1) Pre Poly 1 - From Wafer dispatch to STI Anneal
2) Pre Poly 2 - From HNwell Mask to PWell Anneal RTP
3) Poly - From MVGate Pre Clean to Poly Etch
4) Post Poly 1 - From Poly ReOx Pre Clean to Spacer Nitride Etch Resist Strip
5) Post Poly 2 - From NSD Mask to ILD CMP
6) Backend - From Contact Mask to Top IMD CMP.
7) Final - From Top Via Mask to Finish Good

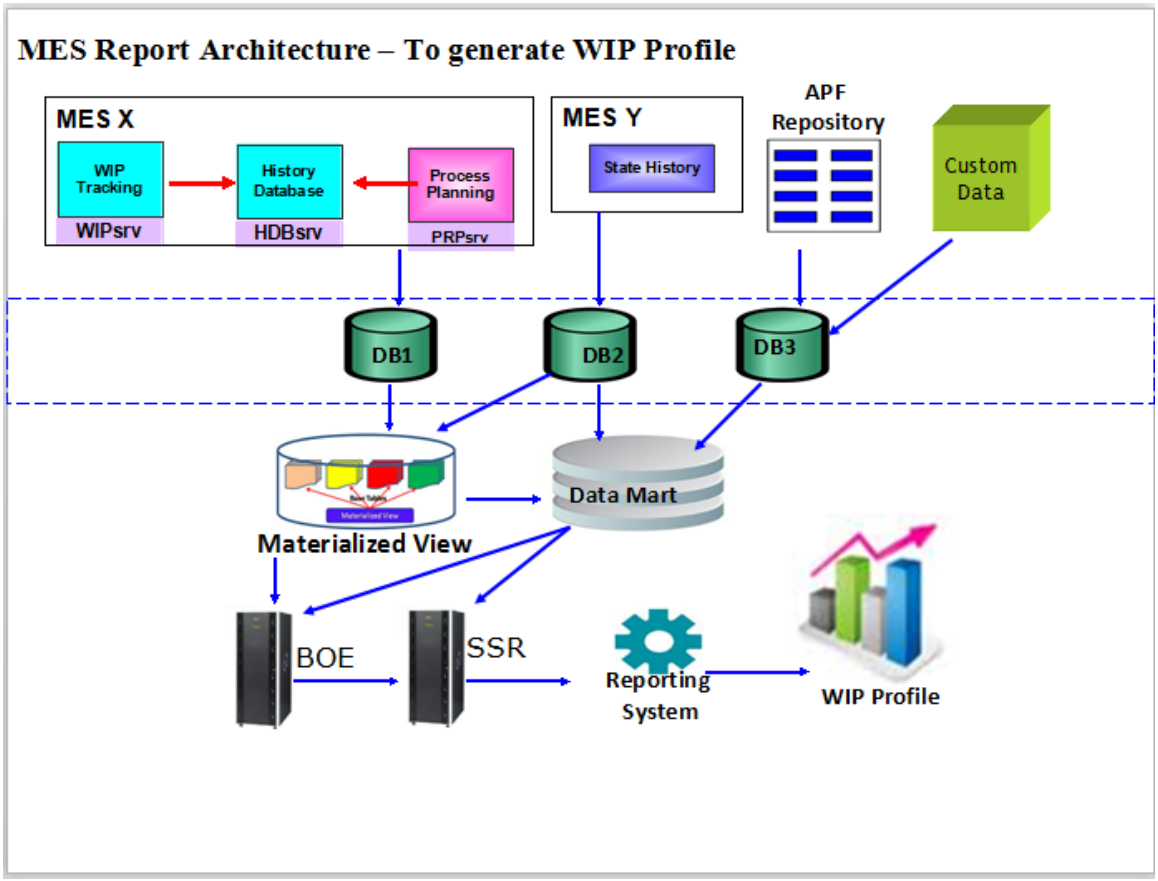


Fig. 3 : MES Architecture in Developing the WIP Profile Report

C. The New WIP Profile Management Methodology

The FAB WIP is divided to 7 sub areas for better management. Each areas is given the specific target based on:

a) Area WIP level
b) The Area average mask level
c) The Area Moves Plan
d) The Area Turn Ratio
e) The Area CT plan

1) PrePoly One (PreP1)

PreP1 started from wafer loading to the Nitride Strip process. With average 4 masks level a longer CT is expected at Prep1 due to reentrants for Diffusion Furnace process.
Diffusion is a batch process and the process duration from 8 to 12 hours. PreP1 has 6 Diffusion steps.

2) PrePoly Two (PreP2)

PreP2 started from HNWell Mask to Pwell Implant Resist Strip process. PreP2 typically has 10 mask layers mainly the reentrants for Implantation process. The wafers typically moves between Photolithography, Implant and Cleaning. Wafers are moving fasters at this area even though Photolitography is the bottleneck for the FAB.

3) Poly

Poly module started from Gate Oxidation 1 or MV Gate Oxidation process to Poly Etch process. Poly typically has 3 mask layers. Poly also consist 4 Diffusion Furnaces step. Due to the longer furnaces process, the process cycle time at this area is designed to be longer.

4) Post Poly 1 (PstP1)

PstP1 started from the NLDD Mask layer to Spacer Nit Etch. PstP1 also has 8 Implants step with 5 mask layers. The theoretical cycle time is shorter and will generate fast WIP turn.

5) Post Poly 2 (PstP2)

PstP2 started from NSD mask layer to ILD CMP process. PstP2 has 3 mask layers. Consist of 3 Implant mask layers and multiple thin film deposition layers. It is also consist 1 Chemical Mechanical Polishing (CMP) layer.

6) Backend (Backend)

Backend started from Contact Mask to Top IMD CMP. Backend has 9 mask layers and multiple reentrant processes between Photolitography, Etch, Thin Film and CMP. Backend is single wafer processing type of tools. Theoretical Cycle time is faster at backend.

7) Final

Final started from Top Via Mask to Shipping. Final has 3 mask layers. The completed processed wafers required to run through electrical test process. Wafer Acceptance Test (WAT) is a routine run test for every wafer where the wafer will be electrically tested. A test structure is designed at the scribe line to electrically confirm our process. Good wafers will be thoroughly inspected by the Outgoing Quality Assurance (OQA). If there are no abnormalities, the good wafers will be packed and ready for shipment to the customer's location.

D. The Discussion about the New WIP Profile Management

Linear WIP balancing is widely used[22], [23]. But the zonal WIP management is an approach to enhance the current method. The fact that wafers run through reentrants at most of the process, a new systematic way to manage the WIP has been discussed. By having the zonal WIP profile management, we can quick to identify whether the real bottle neck (BN) is really occupied with high WIP.

In a real wafer fab, the material flow is generally nonlinear due to different events such as unpredictable tool failure, batch processing, setup change, process dedication and so on. Thus WIP fluctuation occurs frequently, especially lots pile up in front of tool group during downtime period. In that case lots spend hours, even days in the queue if there is no appropriate scheduling. This accumulated WIP in front of a certain tool group causes WIP imbalance for the whole line, which has great impact on cycle time as well as on time delivery.

Sometimes due to equipment availability issue, and also the process limitation due to tight margin, a temporary BN exist in the WIP profile. Spike WIP can be seen clearly and an orchestrated effort from the Engineering team is required to improve the constraint. A group of engineers and the Manufacturing team will look at the alternative way to improve the situation. A small change in the dispatching system is required by the Manufacturing System team to avoid WIP piling up at the temporary BN areas. The upstream WIP will be channeled to the less WIP areas through the Starvation Avoidance (SA) method.

The higher queue time for the wafers to be processed at the temporary BN will impact the overall FAB cycle time. It will also cause capacity lost if the FAB BN area is idle. A dynamic WIP movement management coming from the dispatching system will be complimented if we know the WIP situation. Having the New WIP Profile management will help the production supervisor to make a quick decision on how to handle the incoming WIP.

II. IMPLEMENTATION AND DISCUSSION

Currently there is no calculation is being done to calculate move target based on cycle time target. Instead currently is based on potential move to be done based on tool available. To ensure lots move according to its cycle time target. If the CT target is 1.90 DPML and total mask is 30.5, the equivalent Total Cycle Time Target in Days is 58 days. The above Target is broken down into Group ie PrePoly1 (PreP1, etc based on cumulative CT target at each step. Stage Move is the "Number of Wafers Completed one stage" Turn Ratio (TR) is defined as the "Number of Stage Completed in one day" Target Turn Ratio (TR)

Target TR is total number of stage in the stage group ie PrePoly1 (PreP1), divided by the total CT target in the stage group. Target Move is the Target TR multiplied with the WIP Quantity.

Each step is assigned with cycle time. This is based on IE calculated CT verified every quarter or as needed.

$$TR_z = \frac{\frac{1}{m}\sum_{j=1}^{m}\sum_{i=1}^{n} Stage_i}{CycleTime_z} \quad (1)$$

$$Overall\_TR = \frac{\sum_{z=1}^{s}\left(w_z \left[\frac{1}{m}\sum_{j=1}^{m}\sum_{p=1}^{n} Stage_p \right]_z \right)}{\sum_{z=1}^{s} w_z \sum_{z=1}^{s} CycleTime_z} \quad (2)$$

Where j is PlanName; i is Stage in PlanName j and in StageGroup z;
p is the Stage from beginning to end in PlanName j and inside StageGroup z;
w is the non-negative weights (in this case WIP)
E.g. Prepoly1 Target TR = 12.7/7.7 = 1.6 turns Overall Target TR = 175.4/58 = 3.02 turns
E.g. Prepoly1 Target Move = 1.6 x 6,950 = 11,120.
Overall Target Move = 3.02 x 48,049 = 145,108

$$Overall\_T.Move = Overall\_TR \times \sum_{z=1}^{s} WIP_z \quad (3)$$

A table of the plan moves and stages for each area from PreP1 to Final is in Table 1. (example)

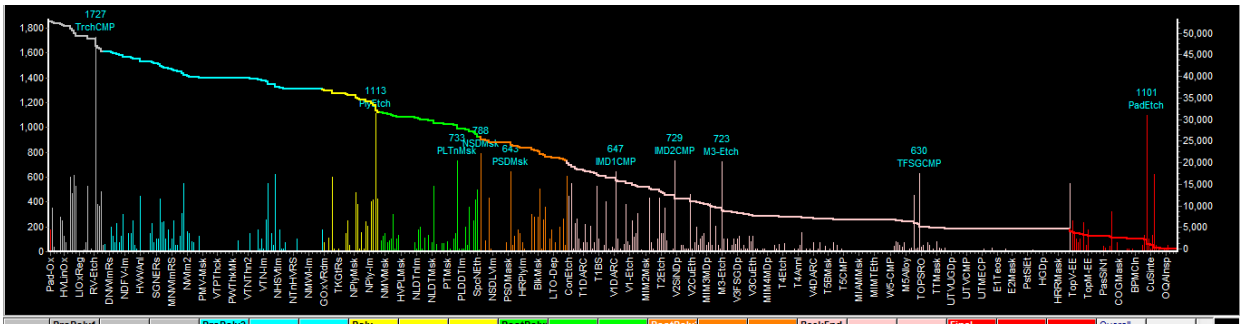
Table 1 : Example of Plan Moves and Stages from PrePoly1 to Final

Area	**PreP1**	**PreP2**	**Poly**	**PstP1**	**PstP2**	**Backend**	**Final**
WIP	6,920	8,958	5,397	5,660	5,525	15,887	4,722
Moves	8,866	38,192	9,814	18,161	14,701	51,546	14,593
TR	1.20	4.20	1.80	3.20	2.60	3.20	3.00
CT (DPML)	1.84	1.82	1.81	1.91	1.98	2.10	2.16
CT Target (Day)	8.34	12.03	6.10	6.13	6.10	14.57	4.00
CT Current (Day)	9.75	11.32	5.72	6.73	7.85	16.45	4.91
Ave Mask	1.50	8.09	2.36	4.02	3.57	8.06	3.17
Cumulative CT (Day)	9.80	21.05	26.80	36.32	44.63	62.94	68.89

Using the dynamic WIP movement, PC and the Manufacturing team are able to forecast the dynamic CT (3) and wafer out plan.

Dynamic CT (DCT) = Total Cumulative CT (Day)/ Total Mask (4)
DCT = Σ day/ Σ mask
DCT = 68.89/ 30.76
DCT = 2.2 dpml

The WIP profile will supplement the information to PC for the line balancing management. Even though the dispatching rule assigned to help move the right WIP or lots, PC able to plan the right moves allocation for each layers by adjusting the rule in the dispatching system. PC can allocate the more moves to the area with higher WIP.
In any case of spike WIP, it will show whether the resource is the FAB bottleneck (BN) or there is other constraint due to tools are not available for production. The WIP will spike up in the WIP profile report if any BN tools down for maintenance or unscheduled.



	PrePoly1			PrePoly2			Poly			PostPoly			PostPoly			BackEnd			Final			Overall	
	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual	Delta	Plan	Actual
EOH		6920			8958			5397			5660			5525			15887			4722			
BOH		7183			8840			5216			5555			5425			16870			4302			
Move	10965	8866	-2099	35817	38192	2375	8924	9814	890	16738	18161	1423	18580	14701	-3879	50173	51546	1373	15425	14593	-832	158000	155873
TR		1.2			4.2			1.8			3.2			2.6			3.2			3.0			
DPML		1.84			1.82			1.81			1.91			1.98			2.10			2.16			
CT_Tgt		8.34			12.03			6.1			6.13			6.1			14.57			4			
CT_Cur		9.75			11.32			5.72			6.73			7.85			16.45			4.91			
Cm_Tgt		8.34			20.37			26.47			32.6			38.7			53.27			57.27			

Fig. 4 : Factory WIP Profile

In Fig. 4, is the example of the WIP profile developed to monitor the line movement. The unbalance WIP movement create issue that may cause low overall FAB moves, high CT, low wafer out and delivery issue to customers.

Based on the WIP profile report in Fig. 4, there are high WIP for Oxide CMP. The WIP spike at Trench CMP, IMD1 CMP, IMD2 CMP and TFSG CMP. These layers are sharing the same resources. To ensure the line balancing intact, PC will plan different moves target for each layers. The WIP profile used for WIP recovery at the spike areas and to meet the monthly moves requirement. PC function is very critical to ensure the right moves plan are incorporated to the dispatching rules. The dispatching rules are flexible for different purposes. This called Moves Target rule. (MT)

In the case of month end, to increase the wafer out plan, PC will increase the moves plan for the backend step. This phenomenal is called 'cut-tail' widely used in Manufacturing activity. To increase the output, PC and Manufacturing team will borrow the following months capacity. In dispatching rule, this is named as Least Remaining Processing Time run first. (LRPT)
This plan will distort the WIP profile. There are potential WIP spike at the front end if the resources are sharing between front end and backend process. In wafer FAB typically, the Photolithography is designed as BN due to the process complexity and cost of the equipment especially the scanners. The process are shared between front end and backend.

PC will have to assign layer moves allocation if the WIP profile distorted to ensure a balancing WIP profile. PC and the Manufacturing team also able to chart each areas performance and do a close monitoring to improve the moves, TR and CT at the respective areas.

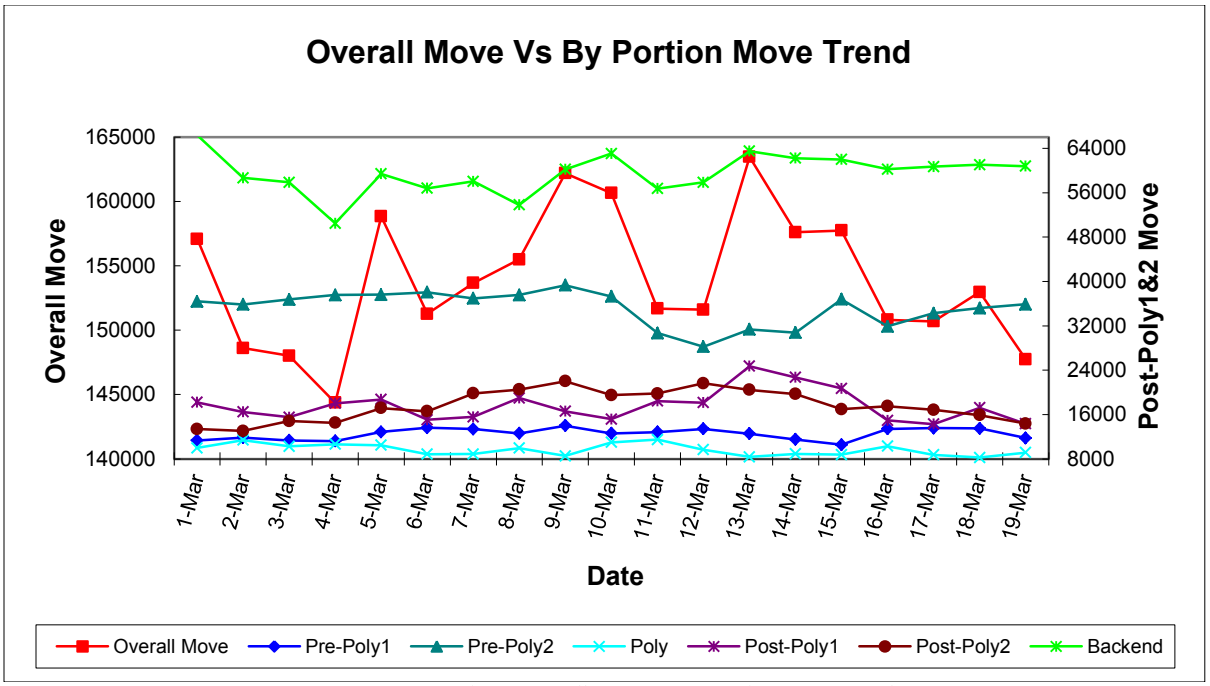


Fig. 5 : Overall Moves vs By Portion Moves Trend

Developing an automated WIP Profile monitoring benefits for the PC and Manufacturing team to monitor the WIP movement real time. Improving the Line Balancing will improve the output of the factory. Based on the factory utilization, the output improve from 3% to 26%. Fig. 6 also shown that the CT trend still intact even though the factory utilization improve. It can be concluded that the 'cut tail' phenomenon or borrowing the future capacity to improve the output do not impact the CT. Even though we use the Least Remaining Step Run First (LRSRF) in the dispatching rules, the CT for the subsequent months are still intact between the factory plan.

The nature of the process and technology in the wafer Fab that process more than 200 devices with different volume at any time, the linear start is not necessary will be a linear output. And it will also not necessary a linear line balancing. It required a close WIP monitoring and having the real time automated WIP Profile report will benefit the PC and Manufacturing team to fine tune the WIP and also the dispatching rules.

Managing the spike WIP and allocating the required output for each process especially that having multiple reentrants process like Photolitography or Implanters are very important for Production Control team activity. They will ensure the Manufacturing team execute the right layers and step . Also not to overdo on certain steps to avoid BN starvation.

Thus having the automated WIP profile report will definitely advantages for FAB WIP monitoring.

Fig. 5 shows the result of the close monitoring on the overall FAB performances especially by the respective areas.

Based on the result after implementing the WIP Profile management, more wafer out was achieved. The company utilization improve > 5% thus more wafer out produced.

This WIP management technique has been implemented since February 2015 and has successfully improve the overall utilization of the Fab more than 100 percent. The utilization is the ratio of the Fab output by the Installed capacity [12]. The formula is wrote in (5).

$$\text{Utilization} = \Sigma \text{ Fabout Quantity} / \Sigma \text{ Fab Installed Capacity} \quad (5)$$

The installed capacity is determined from the bottleneck tool capacity which is in our case located at front-end of the process chain. Thus, there is an opportunity to utilize Fab more than 100 percent by allocate most of the WIP after the bottleneck resources.

The progress result from this technique is demonstrate in Fig. 6. This new technique of WIP management require a month of pre-implementation. This period specifically use to make the PC and Manufacturing team familiar with the systems. A significant result of improvement (41%) on the second month of implementation. The schedule facilities maintenance activity on early and middle of April 2015 impacted the Fab utilization (96%) on April since the product cycle time is within 60 days. Fab managed to recover back on the consequent month (May 2015) and sustained above 100 percent until September 2015.

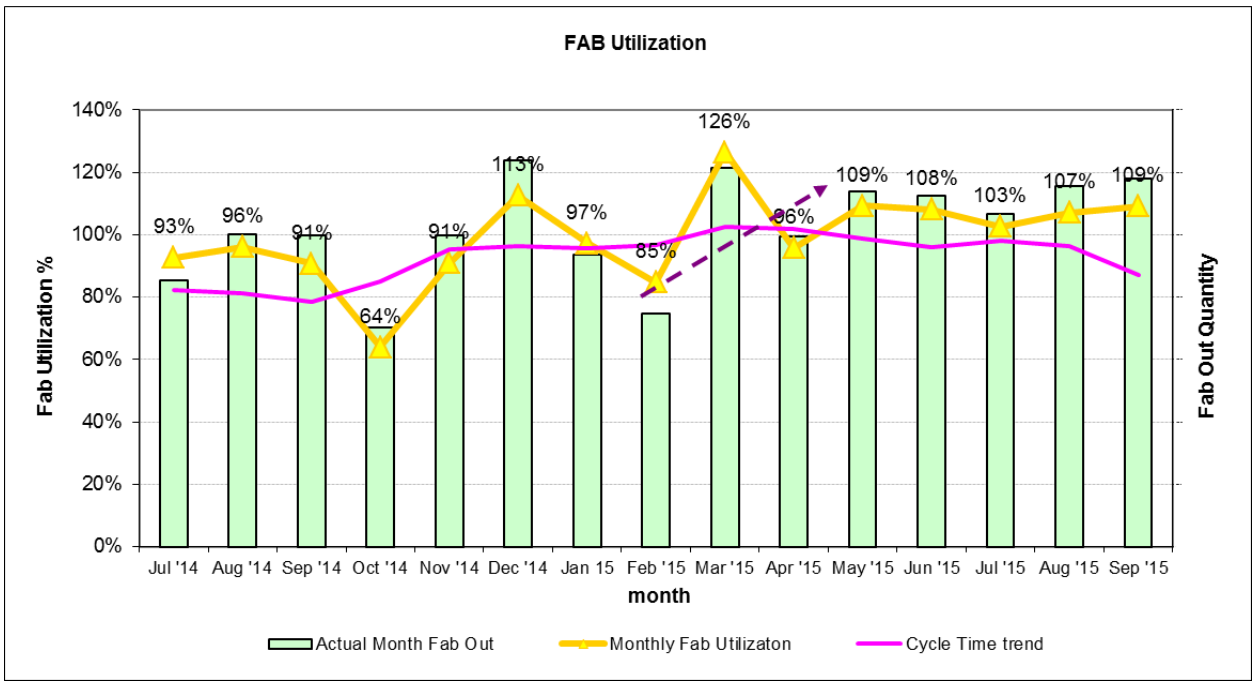


Fig. 6 : FAB Utilization Vs CT Vs Fab Out

III. Conclusion and Summary

Developing an automated WIP Profile monitoring benefits for the PC and Manufacturing team to monitor the WIP movement real time. Improving the Line Balancing will improve the output of the factory. Based on the factory utilization, the output improve from 3% to 26%. Fig. 6 also shown that the CT trend still intact even though the factory utilization improve. It can be concluded that the 'cut tail' phenomenon or borrowing the future capacity to improve the output do not impact the CT. Even though we use the Least Remaining Step Run First (LRSRF) in the dispatching rules, the CT for the subsequent months are still intact between the factory plan.

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IV. ACKNOWLEDGEMENT

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