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Copper Sheet Resistance characteristics in the production staging time limitation study between Copper Seed and Copper Electroplating in Semiconductor Wafer manufacturing

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***Abstract*— Copper metallization in Integrated Circuit interconnect, poses big challenges in Semiconductor Wafer processing. In addition to the stringent Dual Damascene requirement, the Cu material itself is prone to rapid interface diffusion as well as surface oxidation. In production mode, a 12 hours maximum time link has been imposed between the thin Cu Seed deposition to the Cu electroplating step during interconnect depositions. This study attempts to validate the time link requirement through understanding the changes that takes place at different times from sheet resistance perspective in the Cu films. It also looks at the impact of thermal annealing on sheet resistance as a way to compare properties between natural film ageing and applying a forced condition. It is also interesting to correlate sheet resistance changes to other film properties such as reflectance and stress. This study showed the importance of bi-layer in stabilizing sheet resistance stability and the effects of ageing after Cu seed and electroplating steps.**

Keywords—Copper Seed, Copper PVD, Electroplating, Sheet Resistance

I. INTRODUCTION

Copper is extensively used in Integrated Circuit (IC) product due to its low-cost, low-temperature processing requirement [1] and most importantly, low resistivity characteristic. Copper metallization low resistivity application has been a key enabler to the shrinking critical dimensions in today IC technology [2,3]. This is so because Cu has two-fold resistivity reduction compared to Aluminum. It greatly improves the RC delay, critical in smaller geometry and higher performance devices today. However, this advantage comes at a price. Due to its high mobility, element diffusivity and strong surface oxidation tendency, Cu processing is much more complex than Aluminum. Additionally, Cu process and tool sets are more expensive than that of Aluminum[4].

Cu seed process lays out a thin layer of Cu as a seed for the subsequent bulk Cu deposition. Cu seed is deposited via Physical Vapor Deposition process (PVD) while the bulk Cu is deposited using Electroplating process (ECP). In this case, special consideration has been imposed by the tool manufacturer in a form of a maximum time link or allowable time gap of 12 hours between Cu Seed PVD and Cu bulk deposition using electroplating method. Cu seed sheet resistance (Rs) degrades as a function of ageing time is shown in Figure 1. Degradation appears to be at its highest rate in the first 12 hours.

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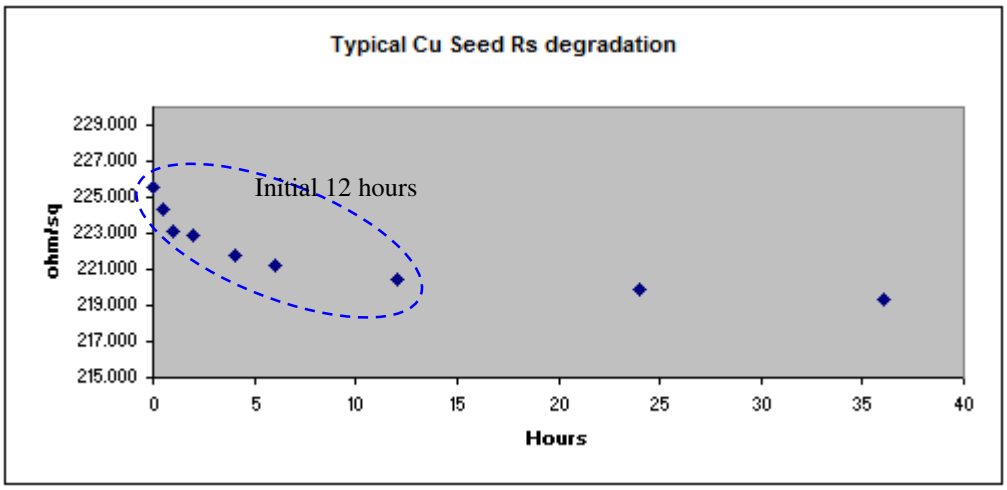

Fig. 1. Rs degradation as Cu seed ages

This study attempts to understand quantitatively the impact of time link on the Cu films sheet resistance characteristics right after seed deposition, after Cu plating as well as after the final Cu anneal steps. It also seek to understand what happens when the TaN/Ta bi-layer film is removed and when anneal is included. Additional parameters, such as Cu reflectance and film stress changes overtime are also reported briefly.

II. Experimental Procedures

A simple illustration of the experimental splits is shown in Figure 2. There are two types of metal stacks which consist of control (Figure 3 (a)) and experimental stack (Figure 3 (b)). Ageing are then subjected to these stacks after Cu Seed deposition (Split A) and Electroplating (Split B) during which measurements are taken at certain ageing intervals; immediate, 0.5, 1, 2, 4, 6, 12, and 36 hours. Simulating the manufacturing steps, anneal is done for each wafer in Split C to see the impact on the sheet resistance. Again bi-layer is removed from the standard stack and aged after electroplating in split D.

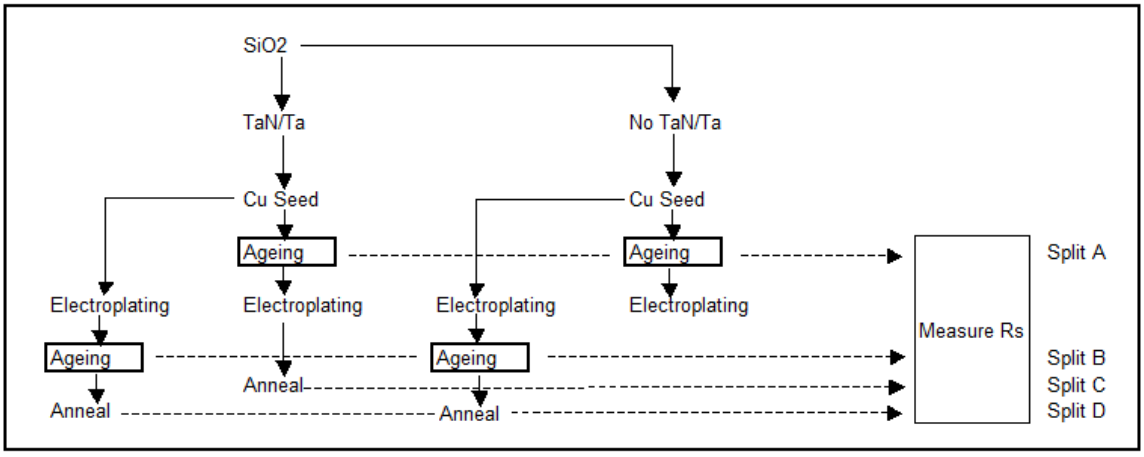

Fig. 2. Overall experiment flowchart

The aim for each split is as follows:

Split A – to access the impact of Cu Seed ageing to Cu seed Rs with and without underlying bi-layer

Split B - to access the impact of Cu Seed ageing to electroplated Cu Rs with and without underlying bi-layer

Split C – to understand the implication on standard stack post anneal Rs when there is ageing after Cu Seed.

Split D - to understand the impact of post Electroplating ageing onto Rs after anneal using the two different stacks

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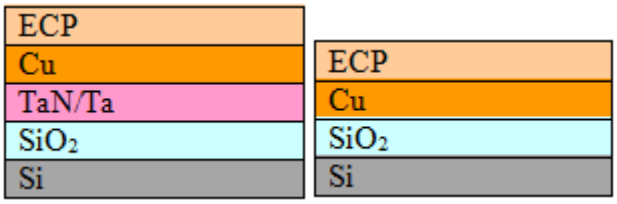

Fig. 3. Stack diagram of prepared samples (a) Stack 1: Standard process with bi-layer ECP/Cu/Ta/TaN/SiO_2/Si and (b) Stack 2: Non-standard process ECP/Cu/SiO_2/Si without bi-layer

All experiments reported in this paper were performed on 200mm wafers. Samples were prepared starting with oxidation of 2kÅ of Tetraethyl orthosilicate (TEOS) was grown on silicon (100) substrate. In a standard sample, after oxidation, a ~200Å thick of TaN/Ta bi-layer was deposited in the Applied Materials Barrier Seed PVD deposition tool. Next, about 1kÅ Cu seed film was deposited in a self ionized plasma PVD chamber. All wafers were processed in the same tool without vacuum break. Annealing was done at about ~180°C for 30 seconds under forming gas at atmospheric pressure. Specimens were aged after Cu seed and Electroplating at various time; immediate, 0.5, 1, 2, 4, 6, 12, and 36 hours. The copper sheet resistance of each specimen was monitored on a four-point probe using OmniMap Rs-100 with 1.6 mil Tip type A and using a 49-point map recipe. Wafers were stored in standard wafer pods under class-100 mini environment all the time when they are not subjected to processing or measurements.

III. Results and Discussion

A. Ageing and Rs trend

The scatter plot shown in Figure 4, depicts the sheet resistance trend for split A. Without TaN/Ta bi-layer barrier (Stack 2), Rs drops rapidly for the first 6 hours and more gradually only after 12 hours. However, only small rate of reduction is seen for standard stack (Stack 1) ageing in the first 2 hours. In perspective, during the first 2 hours, the Rs reduction rates are at 13.9ohm/sq per hour for without bi-layer and 1.31ohm/sq per hour on the standard stack (10x greater rate of reduction). This reduction rates result in 11% and 1.2% lower from the Rs right after seed deposition. After 36 hours, Stack 1 ended up only 2.7% from the initial Rs while Stack 2 at 20%. These phenomenon matches with the observation from other study [5] that TaN/Ta bi-layer has the capability to stabilize the sheet resistance by blocking Cu and SiO2 inter diffusion. Further study is needed to understand the underlying mechanism at work in Rs stabilizing property with the inclusion of bi-layer film. Other studies show that properties Cu and Ta can be changed by modulating ion bombardment and substrate bias during deposition[6,7,8]. Perhaps with this knowledge, better bi-layer property can be engineered and a more robust Cu stack Rs is achievable.

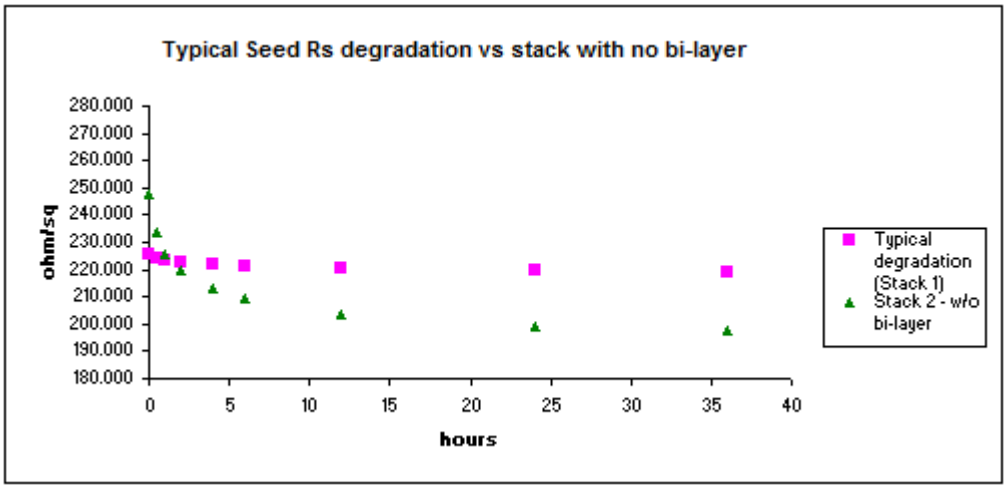

Fig. 4. Sheet Resistance trend of Cu seed ageing with and without anneal after seed ageing

A similar analysis is done for split B. The difference is instead of subjecting ageing to seed layer, it is subjected to electroplated Cu layer. Scatter plot in Figure 5 shows there exist at the initial 4 hours period where Stack 2 (without bi-layer) Rs reduction rate is low at about 0.18 ohm/sq per hour. This follows by an 8 hours of high Rs reduction rate of about 0.5 ohm/sq per hour. As for the standard Stack 1, hardly any Rs reduction is detected. At 36 hours the reduction rate is very minimal at 0.03 ohm/sq per hour. Stack 1 also only scrubbed 3% while stack 2, a whopping 22% from the initial Rs. Similar to the last study, layer with bi-layer effectively stabilize the sheet resistance.

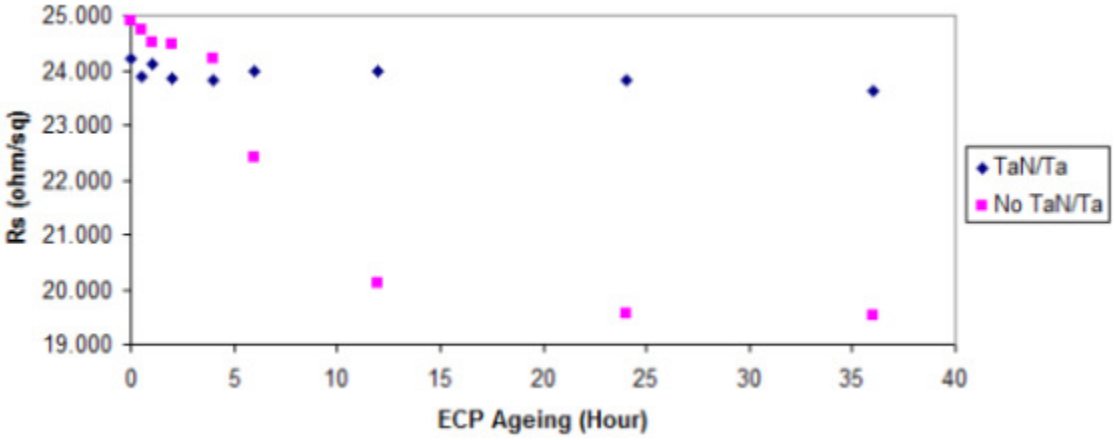

Fig. 5. Sheet resistance of ECP barrier layer splits as left ageing without anneal

B. Post anneal Rs

Post anneal Rs values for split D Stack 1 and 2 are stable (0.07% and 0.05%) at different electroplating ageing times as shown in Figure 6. This is contrary to split B in Figure 5 that shows big difference in Rs stability. Anneal in this case has annulled ageing impact to Rs degradation. During anneal grain growth is accelerated and therefore further growth is minimal. However, Stack 2 has higher average Rs by about 0.5 ohms/sq. The affect of annealing causes intermixing of Cu and SiO2 layers. This study indicates that bi-layer is needed to prevent Cu into diffusing to Si [7,8] causing higher resistance.

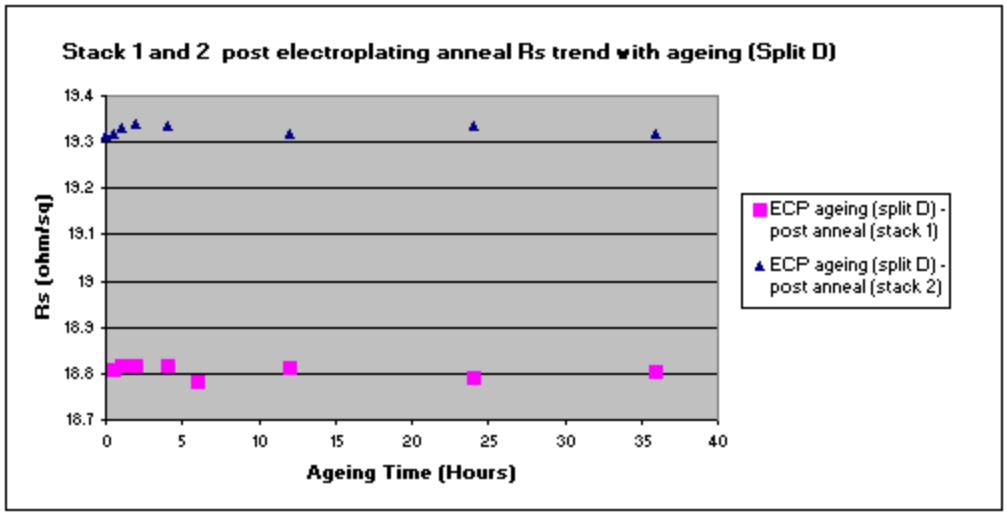

Fig. 6. Post anneal Rs plot showing significant magnitude difference but stable trend at various electroplating ageing times

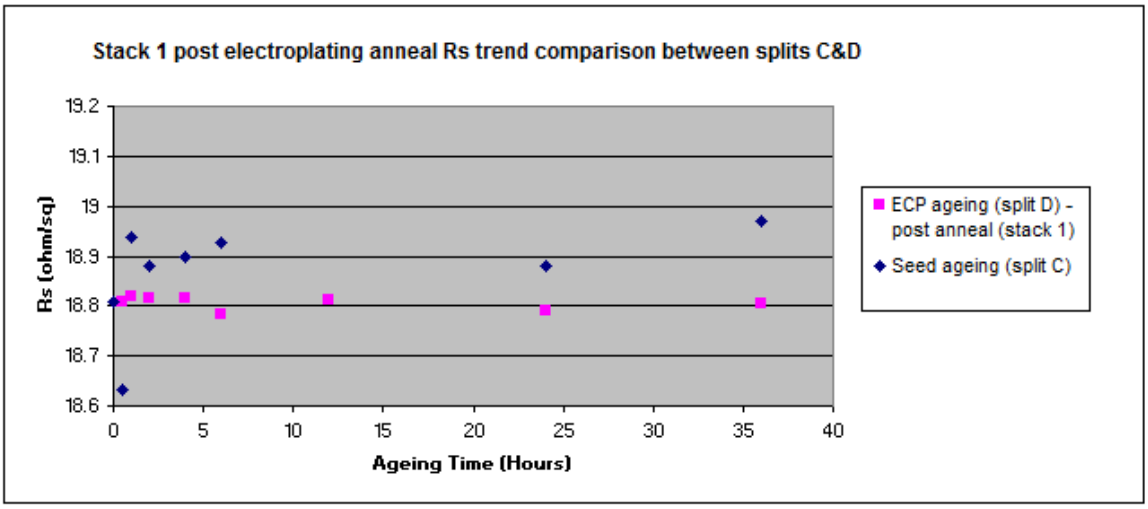

Fig. 7. Higher degree of inconsistency in the seed ageing

Figure 7 compares splits C and D, which ageing takes place after seed and electroplating respectively. Post anneal Rs has very minimal difference (0.06 ohm/sq) with ECP ageing (split D) having the lower Rs. It is interesting to note that ageing impact to Rs inconsistency is more pronounced for seed ageing (split C). compares to ECP ageing (split D). The Rs percent standard deviation is at 0.6%, 20x more than without ageing. Nevertheless, this does not have significant impact to Rs magnitude as a whole compared to study in Figure 6. Future study will include a split with no bi-layer. This is because inconsistencies are seen in both split A and B whenever bi-layer is not present. This will become a really good test on anneal capability to stabilize Rs and annul Cu seed ageing effect. Summary of the overall Rs results is shown in Table 1, below.

Table 1. Overall evaluation matrix and Rs data

Split	Stack	ECP Ageing	Include Biliner	Seed Ageing	Incl Alloy	Rs Measured at	Rs reduction Std dev	Average (ohm/sq)	Rs reduction% std dev	hours to stabilize	stable Rs (ohm/sq)	Remark
A	1		x	x		Seed	2.1	222.1	0.94%	24	219.8	
A	2			x		Seed	16.6	216.7	7.67%	>36	198.0	stable Rs unachieved
B	1	x	x			ECP	0.2	23.9	0.75%	2	23.8	
B	2	x				ECP	2.4	22.7	10.36%	24	19.6	greatest Rs change
C	1		x	x	x	Alloy	0.1	18.9	0.60%	0	-	
D	1	x	x		x	Alloy	0.01	18.8	0.07%	0.5	18.8	
D	2	x			x	Alloy	0.01	19.3	0.05%	0	-	
standard	1		x		x	Alloy	-	19.0	-	-	-	standard/control

In addition to Rs, data of reflectance and stress are also taken at each split. Their standard deviation signifies consistency with average value taken from the entire ageing period. Table 2 below is the summary of reflectance and stress data.

Table 2. Summary for reflectance and stress data

Split	Stack	ECP Ageing	Include Biliner	Seed Ageing	Incl Alloy	Measured at	Average Reflectance	Std dev	Uniformity %	Average Stress	Std dev	Uniformity %
A	1		x	x		Seed	124.9	0.4	0.4%	-0.2	0.0	7.1%
A	2			x		Seed	123.9	0.6	0.5%	0.0	0.0	108.6%
B	1	x	x			ECP	107.4	1.8	1.6%	-61.4	18.0	29.4%
B	2	x				ECP	102.2	2.3	2.2%	1.0	0.2	22.1%
C	1		x	x	x	Alloy	109.2	0.8	0.7%	6.1	0.5	8.2%
D	1	x	x		x	Alloy	100.7	2.7	2.7%	153.5	323.0	210.4%
D	2	x			x	Alloy	102.0	1.1	1.1%	6.0	0.4	7.3%
standard	1		x		x	Seed	129.0	1.7	1.3%	4.8	0.4	7.5%

Correlation plot in Figure 8 shows poor to no correlation between Rs and Reflectance as well as Rs and Stress. Further verification on these two parameters is important as they represent the change in film properties like grain size and crystallography. However, this is beyond the scope of this study.

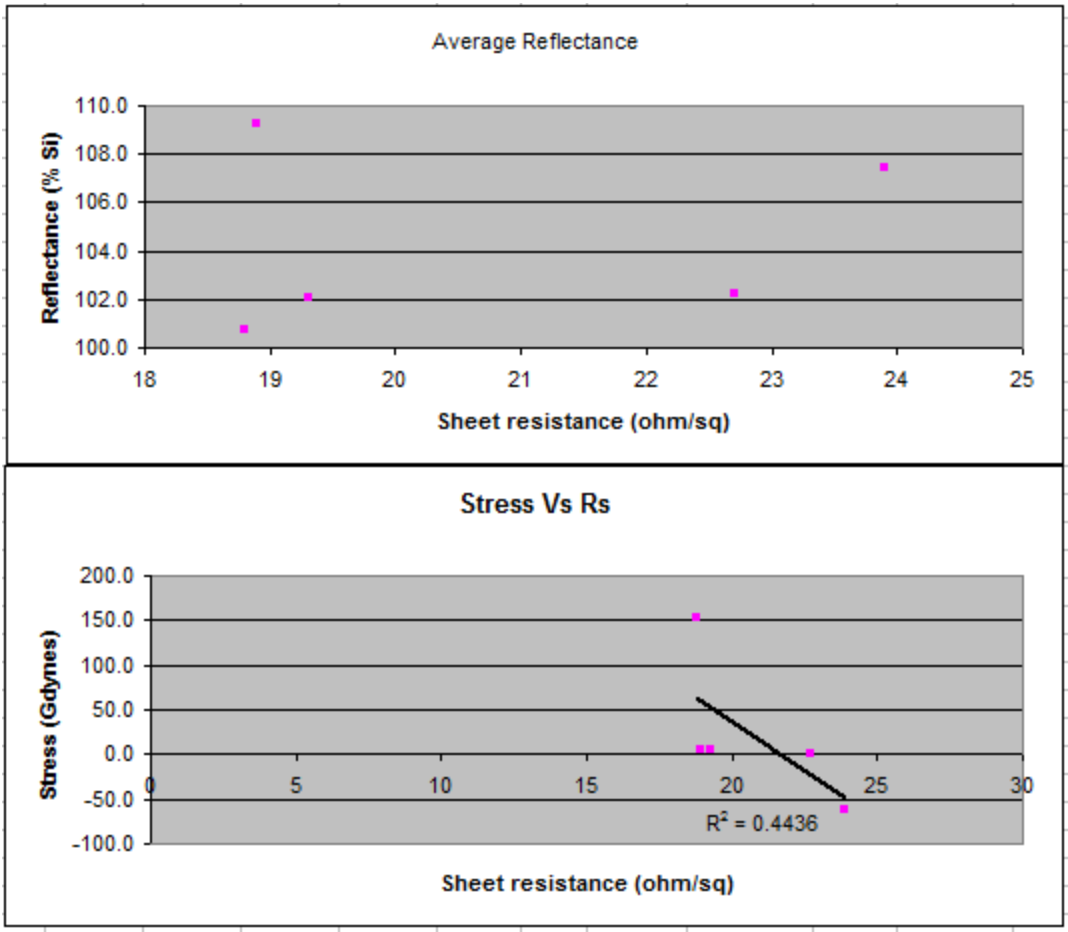

Fig. 8. Scatter plots to understand correlation between Rs to Reflectance and Stress

IV. Conclusion

Bi-layer has the highest impact to Rs consistency in seed and electroplated layer before anneal. It also greatly influences the post anneal film final Rs. Ageing impact can be mostly negated with an anneal step although seed ageing has shown higher impact in post anneal Rs more than ageing after electroplating.

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References

[1] F. Wei, L. Li, and L. Liu, "Facile Synthesis of Copper Nanostructures through Simple Replacement Reaction," IEEE-NEMS 2015, pp. 160-163, April 2015.

[2] J.-W. Lim, Y. Ishikawa, K. Miyake, M. Yamashita, and M. Isshiki, "Influence of Substrate Bias Voltage on the Properties of Cu Thin Films by Sputter Type Ion Beam Deposition," The Japan Institute of Metals. Materials Transactions, vol. 43, no. 6, pp. 1403-1408, Jan. 2002.

[3] R. W. Vook, "Electrical Control of Surface electromigration damage," Elsevier. Thin Solid Films, vol. 305, no. 1-2, pp. 286-291, Aug. 1997.

[4] Larry Pryor, Rick Schlobohm, Bill Brownell, "A Comparison of Aluminum VS. Copper as Used in Electrical Equipment," GE Consumer & Industrial, pp. 1-7.

[5] Y. I. Wanbing, W. Daxiang, L. Kemao, Z. Shaoqiang, and J. B. Tan, " Impact of Pattern Density on Copper Interconnects Barrier Metal Liner Integrity," IEEE Trans. Electron Devices, pp. 289-292, 2014.

[6] D. Edelstein, C. Uzoh, C. Cabral, P. DeHaven, P. Buchwalter, A. Simon, E. Cooney, S. Malhotra, D. Klaus, H. Rathore, B. Agarwala, and D. Nguyen, " A high performance liner for copper damascene interconnects", IITC, pp. 9-11, 2001.

[7] L. Y. Yang, D.H. Zhang, C.Y. Li, P. D. Foo, "Comparative study of Ta, TaN and Ta/TaN bi-layer barriers for Cu-ultra low-k porous polymer integration", Thin Solid Films, vol. 462-463, 176-181, 2004.

[8] M. Thomas, A. Farcy, E. Deloffre, M. Gros-Jean, C. Perrot, D. Benoit, C. Richard, P. Caubet, S. Guillaumet, R. Pantel, B. Chenevier, J. Torres, "Impact of TaN/Ta copper barrier on full PEALD TiN/Ta2O5/TiN 3D damascene MIM capacitor performance," IEEE Trans. Electron Devices, pp. 158-160, June 2007.

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