Semiconductor Fabrication Strategy for Cycle Time and Capacity Optimization: Past and Present

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***Abstract*—This paper investigates the improvements done in capacity and cycle time in semiconductor fabrication foundries. The study will summarize all the techniques, method and know-how used by various foundries to achieve optimum capacity and cycle time. This is important since in 2011, IC Insight reported that the semiconductor content in electronic systems growth was 25% compared to 12% in year 1989. The global semiconductor market has grown 4% for the first three quarters of 2013 compared to a year ago. The trend shows increasing demand and need for continuous focus for improvement in capacity and cycle time. In recent literatures, there is a big gap in cycle time requirement by ITRS versus actual performances by foundries. Study shows a cycle-time gap of up to 30 days. Some of the customers need to wait for additional 30 days for their chips to be fabricated in the wafer fabrication factory. The continuous growth in demand is forcing foundries to re-look at how to improve cycle-time and capacity without spending on new tool purchases. The constraint at wafer fabrication foundries are opening doors for more collaboration and discussion on how to improve the situations. A total of ten projects were evaluated and this paper will summarize the key findings from literatures for potential implementation and to be used as guide for future improvements.**

Keywords— cycle time; capacity; wafer fabrication; semiconductor

I. INTRODUCTION

The invention of the integrated circuit (IC) by Jack Kilby in 1958 drove semiconductor sales growth of 15% per year for four decades [1], [2]. The first customer was the US Air Force and growing industrial and consumers markets drove sales. In the nineties, the personal computer boom drove commercial sales, semiconductor fabrication was always one of the constraints in the supply chain. DRAM, microprocessor and supporting chips were fabricated by the OEM and are migrating to foundry for better cost controls, more capacity and better cycle time to meet the market demand. At the same time, growing demand for consumer goods such as cell phone, walkman, DVD player and mp3 player continue to drive sales . Today in the market, the constraint in the overall supply chain lies in the capacity of the semiconductor fabrication plant to fabricate chips on the wafer [3], [4]. Wafer fabrication is a series of process that make layers of circuits to make transistors and other electrical devices such as capacitors, inductors, resistors to complete the electrical function of a circuitry[5]. Lithography masking layer is where the circuit pattern is transferred from the the mask to the wafers. A normal communication product using 0.18µm technology may have 22 to 26 masking layers [6]. Total wafer fabrication cycle time can range from 30 to 60 days with 300 to 900 steps, of which 30% are re-entrants to the same equipment depending on recipe complexity. The processing of wafers involves changing of material such as chemical and gas to deposit certain material on a wafer [1], [7].

A new 200mm semiconductor fabrication facility that cost US$1 billion in year 2000 is able to produce 30,000 wafers per month using technology ranging from 0.13µm to 0.18µm [4][8]. The investments of US$1 billion to setup the facility for semiconductor fabrication is mainly due to the challenge in the process complexity requirements, high technology equipment set and long lead time [9]. The huge investment and complexity drives the researchers to optimize the manufacturing workflow, improve the equipment performance, increase the product quality and increase capacity.

In semiconductor fabrication, cycle time is measured in days per mask layer or commonly known as DPML[10]. This definition is widely used by many semiconductor references includes FabTimes, Sematech, International Technology Roadmap for Semiconductors (ITRS), IC Knowledge and many more publications that is related to cycle time improvement for semiconductor fabrication. The cycle time in DPML can be represented using equation (1) below:-

$$\text{Days per mask layer [DPML]} = \text{total cycle time in days} / \text{total masking} \quad (1)$$

For example, if a product finish the total processing steps in 43 days and total masking layer is 24, the cycle time in DPML by applying equation (1) is 1.79 DPML. The smaller DPML is desirable and it means faster cycle time.

In 2000, ITRS published the cycle time roadmap for semiconductor fabrication in Factory Integration section for 200mm wafers. The target given for normal production lot was 1.8 DPML for 180 nanometer (nm) technology node. Thereafter, ITRS guidelines no longer publish 200mm technology node roadmap. ITRS shifted focus to 300mm wafers instead and newer technology at 130nm and beyond for new cycle time target[10]–[12]. 1.5 DPML was reported in the ITRS 2011 update [10], [12]. 1.3 DPML was reported in Integrated Circuit Economics 2010 Edition as the best cycle time for normal product for 300mm and 2.5 DPML as average [13]

In year 2010, actual survey claimed by IC Knowledge shows 300mm wafer fabrication performance is at 2.5 DPML. The number show gap of 1 DPML compared to ITRS roadmap 2010 updates. The gap of 1 DPML may range from 20 to 40 days depending on the number of mask layers the product has. In year 2011 Gartner reported that smart-phone grew 72%[14], [15]. Further report from Gartner indicates that the shortages continued to affect popular components, such as camera modules, touch screen controllers, and active-matrix organic light-emitting diode (AMOLED) screens in the fourth quarter of 2010. "This situation will not ease until at least the second half of 2011. Shortages will be a long-term consideration for mobile device vendors, because other fast-growing categories of connected consumer devices, such as media tablets, are competing for the same components," said Ms. Milanesi, research vice president at Gartner[15] . In June 2010, Apple reported the delay of the new iphone 4. Apple claimed unexpected challenges at manufacturing site. The model will be only available in the second half of 2010, about 30 days delay to the market [16]. The smartphone and tablet business continue to be the major driving force in the overall semiconductor space [17]. Again, in year 2012 a report from smart-phone customers like Verizon, AT&T, T-Mobile and Sprint suggest that the new Samsung S3 release in US was delayed by almost 30 days. For example, Verizon original release date was on June 12th, 2012 and actual release was on July 10th, 2012 [9]. The opportunity to improve delivery of the product to meet market demands continues and the research for any opportunity for cycle time improvement continues. This paper will discuss strategies that was applied in the past and present, and validate the new proposal for cycle output optimization strategies.

II. CYCLE TIME VERSUS UTILIZATION

In 1997, the manufacturing strategy is to establish a dispatching systems. Popular theory for scheduling such as Critical Ratio, least SLACK and earliest due date are part of the practice in FAB 2A, Taiwan Semiconductor Manufacturing Company (TSMC) [18]. The challenge was to provide accurate remaining cycle time in the dispatching rule formula[18] . To get the accurate remaining cycle time, amount of lots to be queued and the equipment status must be considered. This paper use the approach to achieve the goal by using historical data in the database as baseline and formula that derived from Little's Law formula[19].

$$N = \lambda T \qquad (2)$$

Where N is the average inventory level of a queuing system, λ is the arrival rate, and T is the cycle time of the system which is exponentially distributed. In other hand, Little's Laws equation provides :-

$$N = u[1 + uV/2(1 - u)] \qquad (3)$$

Where N is the average inventory level or WIP level, u is the equipment utilization, and V is the manufacturing operation and capacity variability, which is equipment availability, efficiency for the operators and others that impact to manufacturing operation. If the two equations combined, then it becomes :-

$$N = \lambda T = u[1+uV/2(1-u)] \qquad (4)$$

Since average processing rate is proportional to equipment utilization u, cycle time can be modelled as:

$$T = a + b[u/(1 - u)] \qquad (5)$$

where (a, b) are coefficients related to fabrication operation and capacity variability that can be estimated from the cycle time versus utilization chart. The cycle time improvement can be done through dispatching policies only using accurate estimation of remaining cycle time.

In 1999, Martin published on the relationship of X-factor towards the overall throughput, or another terminology used by TSMC-IBM called Short Cycle Time Manufacturing (SCM) to help understand and measure the components of line performance and capacity loss[20]. The fundamentals of SCM is that each equipment and process group can be described by a curve relating to normalized cycle time (X-factor) to throughput and that the position of this curve is determined by the capacity loss components. Fig. 1 shows this curve. The similar curve was plotted by Wang et al. 1997 and Chik et. al[18], [21]. The X-factor of each work center is determined by the ratio of actual throughput to the planned capacity. Therefore, if the X-factor is higher than the planned value, results in less idle with no WIP. This occurs when either the throughput is greater than the plan or the capacity is less than the plan.

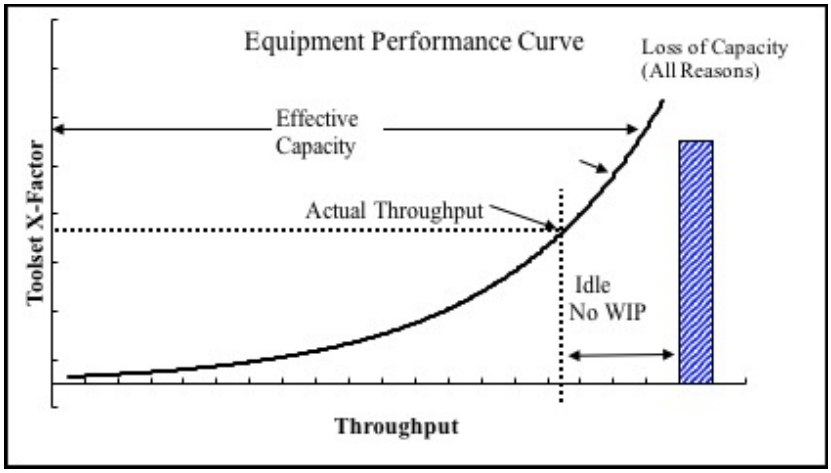

Fig. 1. Equipment performance curve [20].

The default X-factor is defined as the cycle time (CT) divided by the total raw processing time (RPT) of the manufacturing line as follows :-

$$X \text{ (default)} = CT/RPT \qquad (6)$$

The overall line X-factor can be expressed as the sum of the terms found by multiplying the tool/tool set X-factor by the fraction of the total raw process time spent in each too1 set. Further relationship of the equation is expressed by equations 7, where N is the total number of equipment group.

$$X = (CT/RPT) \times Xi, \text{ where } i = 1,2,3 \ldots N \qquad (7)$$

Through this, the expected cycle time with queue time can be defined. To illustrate the equations another literature that expands the topics of cycle time and equipment utilization curve was the paper authored by Delp et. al in the research relating to how X-factor measurement improves cycle time and cycle time variability, published in year 2006 [22]. The paper talks about how the rate at which the cycle time increases is dependent on the system's variability. The cycle time will increase when the utilization rate has passed a threshold level. In most studies this level is between 80-90%. Fig. 2 shows the relationship between cycle time and utilization. Depending on the fab, a balance must be there between cycle time and utilization in view of product to market complications. Late to market means losing the market, but if the utilization is low will mean loss of productivity which translate to loss of income.

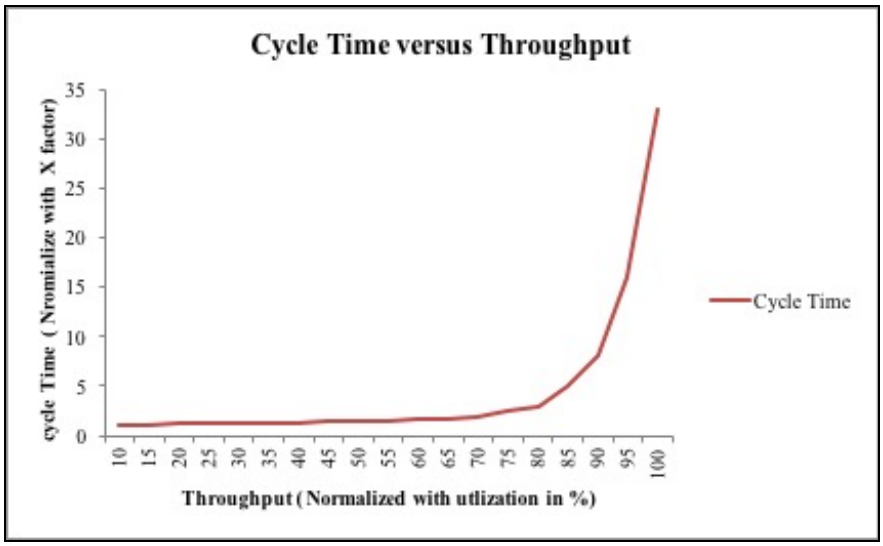

Fig. 2. Cycle time versus throughput. Similar equations have been published by other researchers [22].

III. IMPACT ON PRIOTIZATION

Literature from past analysis shows many techniques to improve monthly output. One of the methods is through sampling for metrology measurement and electrical testing [7]. Other method that also discussed is through improvement in process cycle time or increasing wafer per hour (wph) or delay the equipment preventive maintenance schedule, within permissible time window. Due to the fast evolvement of consumer products, the product change frequency is high and time to market is key to success. Due to this, demand for very short cycle time is inevitable. When customers request for such treatment for a given quantity, then the fab manufacturing respond by having hot lots in the line. These lots will get preferential treatment and move faster and jump queue at most of the workstation.

Fig. 3 shows the cycle time spread without any hot lots in the production line. The spread is reasonable between 75 to 110 days for 95% of the wafers. Fig. 4 shows the cycle time when 3.7% hot lots are introduced in the line. The cycle time spread is wider. Fig. 5 shows that as the number of priority lots increases to 16.7%, then the overall cycle time for regular lots increases to 100 days with a standard deviation results of 11.8 days. The study of hot lots demonstrates that introducing hot lots deteriorates the service level for regular lots, or increases inventory costs. The reason for most fabrication managers to prioritize specific products is to ensure faster cycle time [23]–[25], which helps achieve customer due dates, process improvements, qualify new customer products, and other operational urgent and strategic requirements [26]. High priority products have a shorter cycle time and can run faster than normal production in queue. The hot lots in the production must be controlled to strike a balance between customer request and fab performance

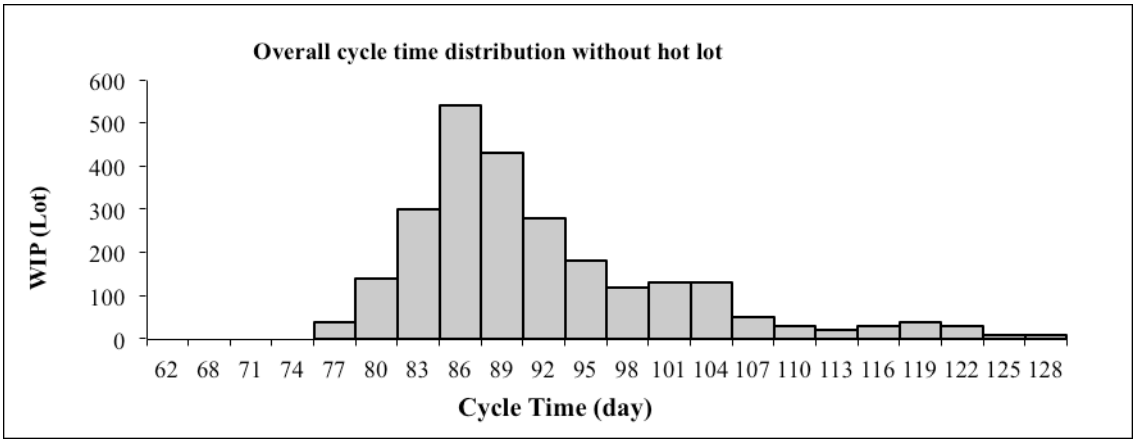

Fig. 3. Overall cycle time distribution without hot lot [23] [27].

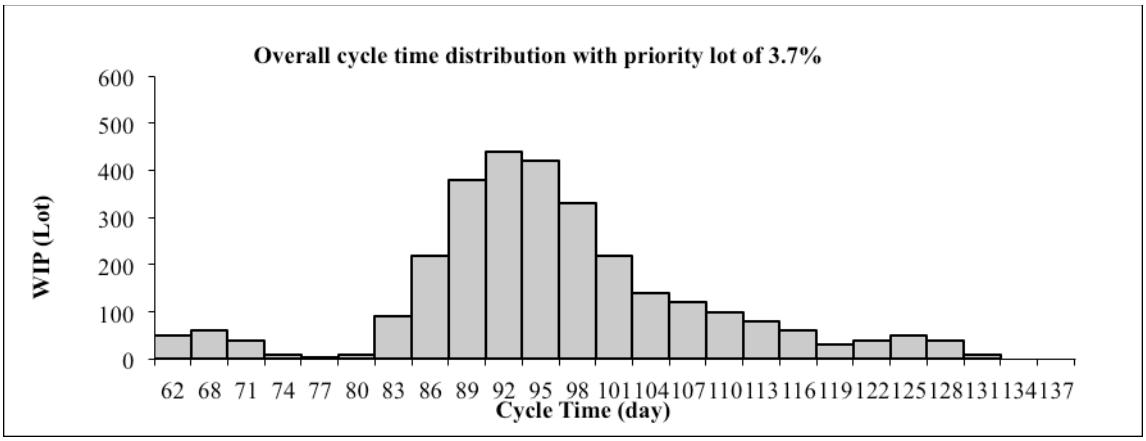

Fig. 4. Overall cycle time distribution with priority lot at 3.7% [27].

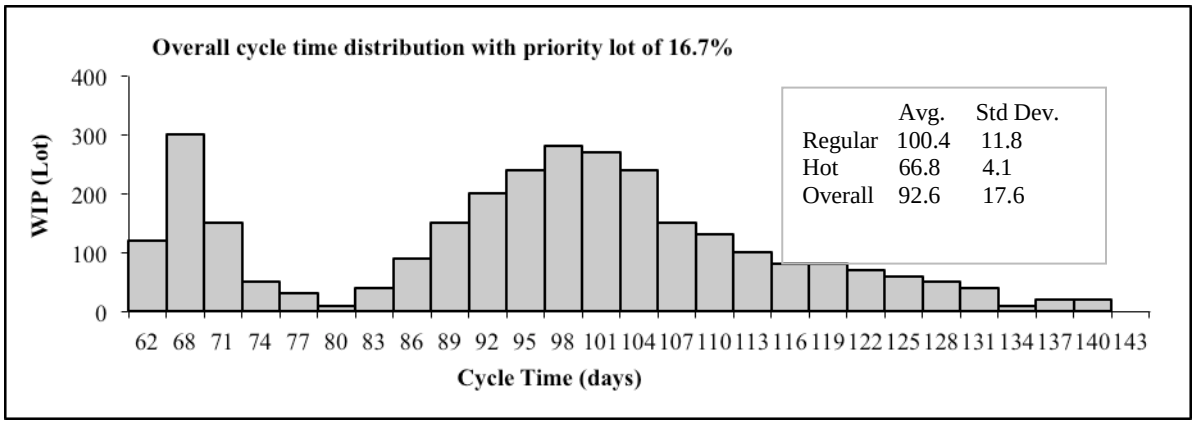

Fig. 5. Overall cycle time distribution with priority lot of 16.7% [27].

IV. Application of Dispatching Techniques for Cycle Time Improvement

Another study of cycle time improvement in semiconductor manufacturing was performed at Inotera Memories Inc., a wafer fab manufacturer of memory devices [28]. Their research reduced the waiting time for WIP, from single processing dry etch equipment to wet equipment, that was waiting for incoming WIP to form proper batch size, because the diffusion furnace process step requires batches of the same recipes to be fully utilized for operational costs [29]–[33]. Most of the processing steps are at the very front-end in wafer manufacturing [34]–[36]. If the same was applied to CMOS products, the improvement may not be effective due to the processes are at very early stage.

The improper batch size problem arises when incompatible product mix arrive first at the batch equipment, with different recipes requirements and disrupt the formation of a complete batch. In this situation different products or technologies, require different process recipes [37]. Because of process and cost requirements, equipment is designed to process a lot in intervals and batches, which needs optimal scheduling approaches, commonly known as complex scheduling in semiconductor fabrication [28], [38]. The primary analysis to this type of scheduling is linear programming, which includes variables for batch size, queue time, material transportation time and integrated with various applications used in semiconductor fabrication facilities such as IBM ILOG, OPL and CPLEX [29].

In this approach, the dispatching policy is centered at the furnace processing state to pull the processing of wet bench. When a batch in a furnace has 60 minutes of processing time remaining, a pull signal is sent to the wet bench machine group, which uses four lots or pods of the same recipe for processing. The 60 minutes setting is conservative to ensure the satisfaction of queue time constraints, but may reduce machine utilization. The authors claimed this approach was tested in a 300mm production facility, and successfully improved utilization of the batching equipment by 10 – 15% and reduced overall lot waiting time by nearly 50% [28]. Since the furnace is not the major production constraint for a typical fab [33], [34], the signifcant results from the analysis are doubted.

Most pure play foundry facilities concurrently fabricate and process more than 30 products for 10 or more customers. The main goal for a foundry is to meet the customers' committed due date with the highest output volume, which helps increase revenue and lower costs. Usually, the responsibility for WIP management rests with the manufacturing operations teams who ensure all the necessary commitments are met through shop floor dispatching. They decide what to process first and which equipment is needed for the products to be processed. These decisions become critical when the WIP is high because different product mix have different processing times and customer due dates.

Seminal work by Nahmias (2004) produced production and operation analysis controls, that focused on shop floor dispatching policies, such as first in first out (FIFO), shortest processing time (SPT), earliest due date (EDD), shortest remaining cycle time (SRPT) and also due date critical ratio (CR). The 4 dispatching policies is the baseline for overall scheduling techniques worldwide [39], [40]. The formula summarized from Nahmias (2004) to calculate due date criticality (CR) is

$$CR = \left[\frac{DueDate - CurrentTime}{Remaining\_Overall\_CycleTime} \right] \qquad (8)$$

The equation should be validated using proper results analysis, which can be generated from real time dispatching (RTD) systems that select wafer processing equipment. RTD systems are UNIX programs that use dispatching rules to serve respective manufacturing operation objectives, and are commonly found in wafer fabrication foundries [41]. The results from this approach differ depending on the bottleneck equipment. Fig. 6 shows dispatching policy comparisons, where different dispatching policies give different cycle times. The comparison analysis results in different cycle time and output volume depending on foundry capacity settings and process technology requirements because of the many re-entrance processes where the same equipment repeatedly processes products.

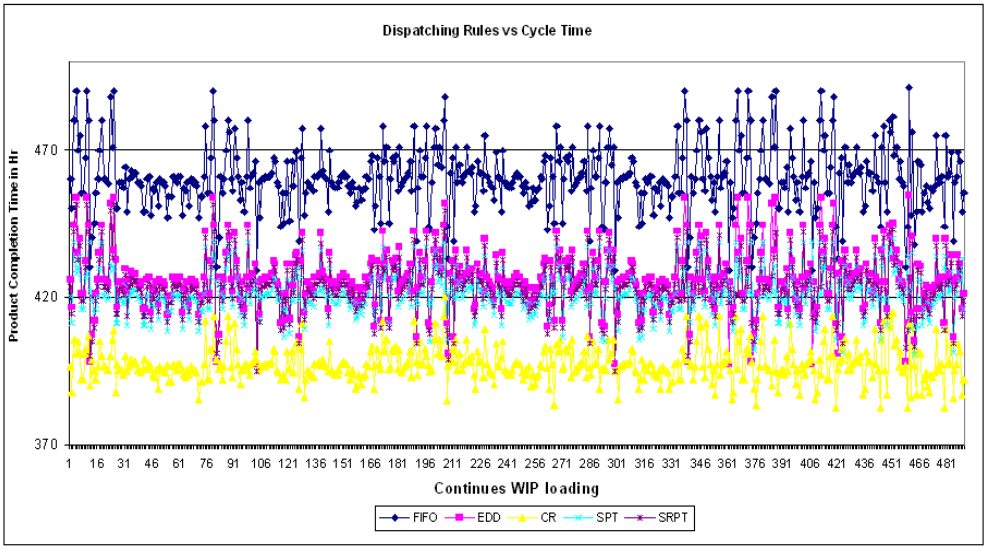

Fig. 6. Comparing dispatching rules for FIFO, EDD, CR, SPT and SRPT [42] [43].

V. Capacity and Cycle Time Improvement with CAPEX investment

The last method reviewed is the recent industry plan to increase capacity and improve cycle time with CAPEX investment. This is documented in a report by Ibrahim, Chik and Hashim (2014), the finding which are summarized in Fig. 8. The most popular methods major foundries use to expand capacity are to acquire an operational fab, purchase used equipment with minor expansion or purchase new equipment with minor expansion, purchase used equipment with new fab or new equipment with new fab. From the information presented in this review, the most effective way to expand fab is by acquiring an operational fab, which was valued at US$5 million for capacity of 1K wafer per month. However, investors need to purchase the total capacity of the fab [44], [45]. For example, if the total capacity of the fab is 40,000 wafers per month, then the total cost is USD 80 million. Another option is to purchase used equipment from the open market or from the equipment refurbisher. This technique was recently implemented at SilTerra during a recent expansion to reduce the bottleneck in capacity for a more advance node [45].

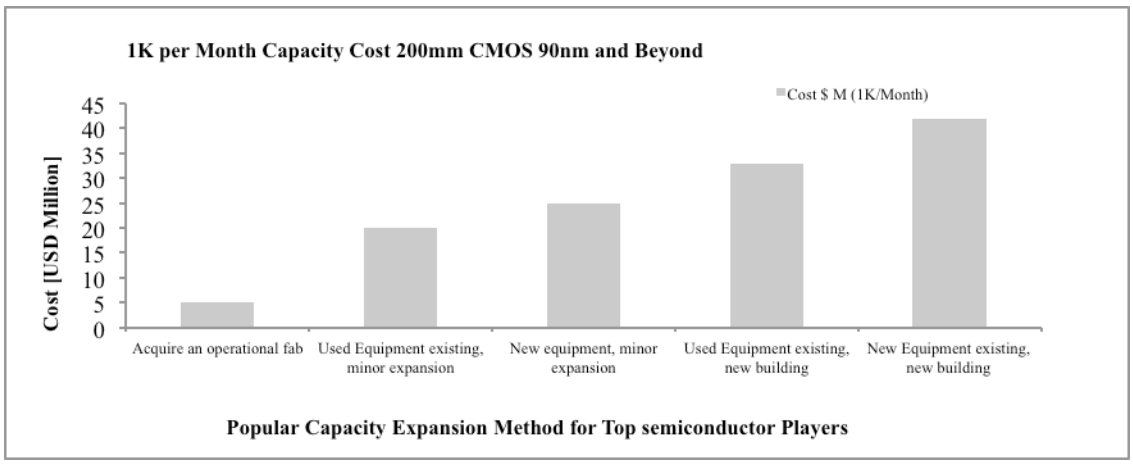

Fig. 7. CAPEX capacity expansion options [45]

VI. Conclusion

This paper investigates the literature on fab capacity and cycle time improvement in semiconductor wafer fabrication. The semiconductor fabrication bottleneck is typically the lithography process. Much of the research into fab capacity increment has focused on equipment related improvements, such as improvements in equipment up time, faster processing recipes, reducing the frequency of preventive maintenance, finding the optimum schedule for preventive maintenance or expediting the preventive maintenance. Examination of more literatures in scheduling techniques such as batching concepts that improves the efficiency of the process and processing equipment. The capacity improvements can be significant; as high as 8% for individual piece of equipment. If the assumption is that the equipment is the constraint, potentially fab capacity can increase by 8%. While theoretically this helps improves capacity, but benefits may take three to six months to materialize. This will be a smooth plan if the demand is confirmed, but this does not happen because demand is unpredictable [17], [46]–[49].

Another area that has contributed to incremental output is the reduction in cycle time through improvement in scheduling and dispatching. Improper cascading leads to low efficiency, which indirectly impacts capacity.

If all the activities were done and the capacity needed is not achieved, then fabs have no choice but to resort to CAPEX (capital expenditure) spending. There are many ways to approach this method as shown in fig. 7.

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REFERENCES

[1] M. A. Chik and U. Hashim, "Study of the Cycle Time Behavior for product scaling 0 . 16um and smaller in Foundry," in *International postconferenceconference*, 2010, pp. 2–5.

[2] K. Jack S, "Turning Potential into Realities: The invention of the Integrated Circuit," *Texas Instruments*, Dallas, pp. 474–485, Dec-2000.

[3] K. Ibrahim, M. A. Chik, and U. Hashim, "Managing Demand Variability to Achieve Optimum Cost and Revenue in Wafer Foundry," 2010, no. December, pp. 7–10.

[4] M. A. Chik, K. Ibrahim, M. H. Saidin, F. Yusof, G. Devandran, U. Hashim, and J. K. Setar, "Development of Capacity Indices for Semiconductor Fabrication," in *International conference of semiconductor Electronics*, 2012, pp. 684–688.

[5] N. Muhammad, J. Chin, S. Kamarrudin, M. Chik, and J. Prakash, "Fundamental simulation studies of CONWIP in front-end wafer fabrication," *J. Ind. Prod. Eng.*, vol. 32, no. 4, pp. 232–246, 2015.

[6] H. A. David, "Increase Fab Capacity Scheduling with Predictive Short-interval," in *Advanced Semiconductor Manufacturing Conference*, 2011, pp. 1–4.

[7] P. Balakrishna, M. A. Chik, I. Ahmad, and B. Mohamad, "Throughput improvement in semiconductor fabrication for 130 µm technology," *2011 IEEE Reg. Symp. Micro Nano Electron.*, pp. 228–231, 2011.

[8] K. Ibrahim and M. A. Chik, "Variability Due to Tool Configurations That Impacts Overall Capacity in Wafer Fabrication Facility," in *The 11th Asia Pacific Industrial Engineering and Management Systems Conference The 14th Asia Pacific Regional Meeting on International Foundation for Production Research*, 2010, no. December, pp. 7–10.

[9] K. M. Zain, "Semiconductor fabrication eco-systems and supply chain in Malaysia," *2010 IEEE Int. Conf. Semicond. Electron.*, pp. A8–A8, Jun. 2010.

[10] ITRS, "International Roadmap for Semiconductor (ITRS) 2012 Factory Integration Report," ITRS, Korea, 2012.

[11] ITRS, "International Roadmap for Semiconductor (ITRS) 2001 Factory Integration Report," 2001.

[12] ITRS, "International Roadmap for Semiconductor (ITRS) 2010 Factory Integration Report," 2010.

[13] W. Jones, *Integrated Circuit Economics*, 2010th ed. IC Knowledge LLC, 2010.

[14] J. Rivera and M. R. V., "Worldwide Semiconductor Foundry Market Grew 16.2 Percent in 2012, According to Final Results by Gartner," *Gartner Press Release. 24/4/2013.*, 2013. .

[15] C. Pettey and L. Goasduff, "Gartner Says Worldwide Mobile Device Sales to End Users Reached 1.6 Billion Units in 2010; Smartphone Sales Grew 72 Percent in 2010," *Gartner Press Release. february 9, 2011*, 2011. [Online]. Available: http://www.gartner.com/newsroom/id/1543014. [Accessed: 12-Dec-2013].

[16] E. Ogg, "More than 1M ipHone 4S sold in first day," *GIGAOM*, 2011. [Online]. Available: www. gigaom.com.

[17] SC-IQ, "Tables, smartphones & China still driving growth," *Semiconductor Intelligence (SC-IQ) Newsletter 23/10/2013*, 2013. .

[18] T. Wang, K. Lin, and S. Huang, "Method of Dynamically Determining Cycle Time of a Working Stage," in *International Electronics Manufacturing Technology Symposium (CPMT/IEEE)*, 1997, no. 121, pp. 403–407.

[19] J. D. C. Little and S. C. Graves, "Little's Law," in *Operation Management Models and Principles*, D. Chhajed and T. J. Lowe, Eds. 2008, pp. 81–100.

[20] D. P. Martin, "Total operational efficiency (TOE): the determination of two capacity and cycle time components and their relationship to productivity improvements in a semiconductor manufacturing line," *10th Annu. IEEE/SEMI. Adv. Semicond. Manuf. Conf. Work. ASMC 99 Proc. (Cat. No.99CH36295)*, pp. 37–41, 1999.

[21] M. A. Chik, V. C. Yung, P. Balakrishna, U. Hashim, I. Ahmad, and B. Mohamad, "A study for Optimum Productivity Yield in 0.16 µ m mixed of Wafer Fabrication Facility," in *international conference of Semiconductor Electronics 2010*, 2010, pp. 444–447.

[22] D. Delp, J. Si, S. Member, and J. W. Fowler, "The Development of the Complete X-Factor Contribution Measurement for Improving Cycle Time and Cycle Time Variability," *IEEE Trans. Semicond. Manuf.*, vol. 19, no. 3, pp. 352–362, 2006.

[23] R. W. Wolff, *Stochastic Modeling arid the Theory of Queues*. New Jersey: Prentice-Hall, Inc, 1989.

[24] J. Rothe, R. Barlovi, A. Becker, R. Goss, D. Grossmann, W. Jäckel, S. Knappe, T. Kowtsch, S. Melzig, M. Reiche, U. Schulze, H. Wagner, H. Weindl, and D. Zschäbitz, "Lean Randomization and Exception Handling," pp. 236–240, 2010.

[25] B. Deniz, I. Karaesmen, and A. Scheller-Wolf, "Managing perishables with substitution: Inventory issuance and replenishment

heuristics," *Manuf. Serv. Oper. Manag.*, vol. 12, no. 2, pp. 319–329, 2010.

[26] C. R. Glassey and M. G. C. Resende, "Closed-loop Job Release Control for VLSI Circuit Manufacturing," *IEEE Trans. Semicond. Manuf.*, vol. 1, no. 1, pp. 36–46, 1988.

[27] B. Ehteshami, R. G. Pctrakian, and P. M. Shabe, "Trade-offs in Cycle Time Management : Hot Lots," *IEEE Trans. Semicond. Manuf.*, vol. 5, no. 2, pp. 101–106, 1992.

[28] S. Wang, F. Wang, J. Chang, J. Chang, S. Chang, P. Wang, P. B. Luh, Y. Ka, and S. Zhan, "Optimal Wet-Furnace Machine Allocation for Daily Fab Production," in *18th International Symposium on Semiconductor Manufacturing, ISSM2010*, 2010, p. MCO–119.

[29] M. Mathirajan and A. I. Sivakumar, "A literature review, classification and simple meta-analysis on scheduling of batch processor in semiconductor," *Int. J. Adv. Manuf. Technol.*, vol. 29, no. 9–10, pp. 990–10001, 2006.

[30] D. Babbs and R. Gaskins, "Effectiveness of Small Batch Size on Cycle Time Reduction in a Conventional 300mm Factory," *2007 IEEE/SEMI Adv. Semicond. Manuf. Conf.*, pp. 105–110, Jun. 2007.

[31] Y. M. Tu, H. N. Chen, and T. F. Lie, "Shop-Floor Control For Batch Operation With Time Constrains In Wafer Fabrication," *Int. J. Ind. Eng. Theory, Appl. Pract.*, vol. 17, no. 2, pp. 70–81, 2010.

[32] G. Kenyon, C. Canel, and B. D. Neureuther, "The impact of lot-sizing on net profits and cycle times in the n-job, m-machine job shop with both discrete and batch processing," *Int. J. Prod. Econ.*, vol. 97, no. 3, pp. 263–278, Sep. 2005.

[33] FabTime, "FabTime Dispatching Module," *Cycle Time Management for Wafer Fabs*. 2011.

[34] SilTerra Manufacturing Systems Department, *SilTerra Training Syllabus for Engineer: Introduction to Cycle Time Class Training*, Revision 6. Kulim, Kedah, 2013.

[35] S. P. Bates, *Silicon wafer Processing*. Applied Material, 2000.

[36] M. Wu, W. Wang, L. Tian, C. Wu, and D. Fan, "Leakage in CMOS Devices Induced by Pattern- Dependent Microloading Effect," no. 15, pp. 468–471, 2012.

[37] R. Bixby, R. Burda, and D. Miller, "Short Interval detail production scheduling in 300mm semiconductor manufacturing using mixed integer and constraint programming," in *IEEE/SEMI Advanced Semiconductor Manufacturing Conference*, 2006, pp. 148–154.

[38] M. Ham and J. W. Fowler, "Scheduling of Wet Etch and Furnace Operation with Next Arrival Control Heuristic.," *Int. J. Adv. Manuf. Technol.*, vol. 38, pp. 1006–1017, 2008.

[39] S. Nahmias, *Production and Operation Analysis*, 5th ed. New York: McGraw Hill Higher Education, 2004.

[40] K. Nikolopoulos, A. A. Syntetos, J. E. Boylan, and V. Petropoulos, F. Assimakopoulos, "An aggregate–disaggregate intermittent demand approach (ADIDA) to forecasting: an empirical proposition and analysis," *J. Oper. Res. Soc.*, vol. 62, pp. 544–554, 2011.

[41] S. Q. Yao, Z. Jian, N. Li, H. Zhang, and N. Geng, "A multi-objective dynamic scheduling approach using multiple attribute decision making in semiconductor manufacturing," *Int. J. Prod. Econ.*, vol. 130, pp. 125–133, 2011.

[42] C. Pickardt, J. Branker, T. Hildebrandt, J. Heger, and B. Scolz-Reiter, "Generating dispatching rules in semiconductor manufacturing to minimize weighted tardiness," in *Generating dispatching rules in semiconductor manufacturing to minimize weighted tardiness*, 2010, pp. 2504–2515.

[43] SilTerra Manufacturing Systems Department, *SilTerra Training Syllabus for Engineer:Introduction SilTerra Dispatching List (SDL) Training*, Revision 8. Kulim, Kedah: SilTerra Malaysia, 2014.

[44] M. David, "European equipment CAPEX to grow 50% next year," *ElectronicsWeekly.com*, 2013. [Online]. Available: http://www.electronicsweekly.com/news/business/european-equipment-capex-to-grow-50-next-year-2013-12/.

[45] K. Ibrahim, M. A. Chik, and U. Hashim, "Horrendous Capacity Cost of Semiconductor Wafer Manufacturing," in *International Conference of Semiconductor Electronics 2014 (IEEE-ICSE2014 Proc. 2014*, 2014, pp. 345–348.

[46] C. G. Dieseldorff, "Fab equipment Spending to Rise. Semiconductor Manufacturing & Design Community," 2013. [Online]. Available: http://semimd.com/semi/2013/06/07/fab-equipment-spending-to-rise.

[47] SIA, "Semiconductor Industry Association (SIA) update for Global Semiconductor Sales Increase in October, Remain Above Seasonal Rate," *Semiconductor Industry Association (SIA) Press Release 2012*, 2012. [Online]. Available: www.sia-online.org.

[48] IC Insights, "Global Wafer Capacity 2011-12 Detailed Analysis and Forecast of the IC Industry's Wafer Fab Capacity," *IC Insights Research Bulletin*, 2011. [Online]. Available: www.isuppli.com Semiconductor-Value-Chain/MarketWatch/Pages/IHS-Downgrades-Semiconductor- Market-Outlook.aspx.

[49] D. Ford, "IHS Downgrades Semiconductor Market Outlook—Revenue Decline Now Expected for 2012," *News Release, iSuppli*, 2012. [Online]. Available: www.isuppli.com/semiconductor-value-chain/news/pages/ihs-downgrades-semiconductor-market-

outlook-revenue-decline-now-expected-for-2012.aspx.

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