The Influence of Industrial Engineering in Semiconductor Fabrication Factory Optimization

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***Abstract*— To meet competitive market for the electronics consumer products, the integrated circuit is process at the semiconductor fabrication factory which is the most complex and challenging areas in manufacturing. This is due to semiconductor manufacturers will require to process 300 to 1000 steps depends on products, 60,000 WIP and 400 pieces equipment for typical 200mm wafer size technology. Due to this complexity, the product mixed is highly influence the capacity of the factory. Without careful planning, a product mixed will lead to lower output and resulted to lower revenues. This is very critical due the investment cost is of a factory can reach up to USD 4 billion. Most company would like to optimize the factory as much as possible to ensure fast profit return and to ensure operational sustainability. This paper will discuss how the Industrial Engineers (IE) plays the roles for capacity management to influence the factory output based on case study of semiconductor fabrication company, SilTerra Malaysia. The methodology use for data collection and data verification is from automated systems that integrated with the equipment with real time data transaction then summarized into E10 and OEE approach. This allow more analysis for better decision to decide product mix loading plan for factory sustainability and improvement up to 14.3% of the potential revenue.**

Keywords—Semiconductor fabrication, Industrial Engineering (IE), Work in Progress (WIP), Theory of Constraint (TOC), Overall Equipment Effectiveness (OEE)

I. INTRODUCTION

Semiconductor manufacturing plants are complex environments, extending across multiple manufacturing domains [1], [2]. The process starts with wafer manufacturing, progresses to chip manufacturing, which involves probe/e-test, backgrind, singulation, and finishes in product manufacturing where the final package is assembled and tested (see Fig. 1). Semiconductor fabrication is also at the heart of the electronics supply chain, which makes it susceptible to the same demand peaks and troughs that have been part of the industry since it established itself in the 1960s [3]–[5]. A semiconductor fabrication plant, commonly called a fab, is a clean room manufacturing facility [6]–[8]**.** The typical manufacturing process contains 300 to 1000 steps, depending on product complexity. Much of the complexity comes from the need for wafers to be processed through the same equipment multiple times, especially at photolithography, etching, implanter, film deposition, chemical mechanical polishing (CMP) and cleaning [9], [10]. Table 1, illustrate the product mix complexity based on the technologies ranges, total number of steps, re-entrance steps at litho, etch and metal layers. Typical CMOS 0.11µm to 0.18µm 200mm technology mix at capacity range of 25K to 30K will need 400 to 500 equipment. Far advanced 300mm, newly build wafer fabs have capacity more than 60K capacity and more equipment quantity installed[11], [12] [13].

Nowadays, most chips are fabricated in one of the top 200 or 300mm semiconductor fabrication pure play foundries, such as those owned by Taiwan Semiconductor Manufacturing Corporation (TSMC), United Microelectronics Corporation (UMC), Global Foundry (GF) and Semiconductor Manufacturing International Corporation (SMIC). These organizations have revenues in excess of USD15 billion per year [14]. Cost estimates for a new fab range from one to four billion US

dollars [15]–[17]. For example, chip manufacturer TSMC invested 9.3 billion dollars in its 300 mm wafer manufacturing facility in Taiwan in 2013 [18].

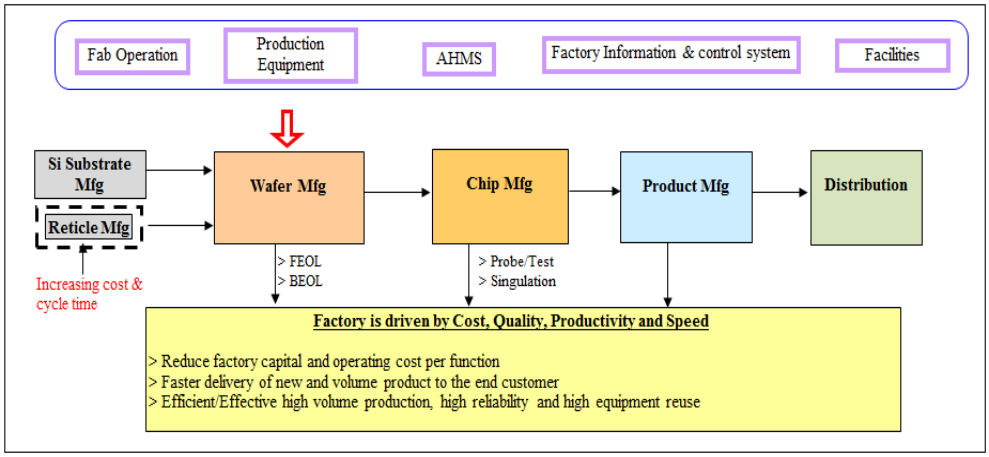


Fig. 1. Overall semiconductor factory integration scope defined by International Roadmap of Semiconductor. Source [2], [19].

Table 1: Example of typical product mixed based on technology, total steps, lithography, etch and metal layers

Product Name	Tech	Total	Litho	Etch	Metal	Allocation
Control_II	0.18µm	510	24	48	4	20%
VID_CC	0.18µm	515	26	52	4	20%
BlueT_OO	0.16µm	567	30	60	5	16%
Smart_WW	0.16µm	670	30	68	5	14%
Toys_RR	0.11µm	821	33	72	7	12%
Touch_CC	0.16µm	550	30	60	5	10%
Control_33	0.13µm	723	34	72	6	6%
Display_ENGR_1	90nm	811	36	72	6	2%
Weighted Avg / Total		603	29	60	5	100%

The key difference between a foundry and integrated device manufacturer (IDM) is the flexibility of processing mixed products at lower production costs [4]. Pure-play foundry fabs have increased revenues over the last 10 years, compared to IDM fabs as a result from IDMs are changing to become foundries, which fuels the need for continuous improvement in foundry fab efficiency. In 2010, AMD announced that its processor manufacture has been migrated from an IDM to foundries owned by Global Foundries [4]. Another change is that Intel and TSMC collaborated on the Atom chip production [20]. Others IT companies such as Broadcom, Qualcomm, and IBM already fabricate their chips in foundries, which supports the market trend towards semiconductor foundries compared with IDM.

In Malaysia, the major foundries are SilTerra in Kulim, Kedah, and X FAB in Kuching, Sarawak [7], [21]. Therefore, the fab process research is limited because there are only a handful of less experienced fab operators who are unable to convert operational gaps into research opportunities. The exploration in this topic enriches our understanding of wafer fab challenges and potential improvements. One of the main strategies SilTerra Malaysia Sdn Bhd is currently researching is how to improve revenue by improving fab capacity that is driven from Industrial Engineering (IE).

II. INDUSTRIAL ENGINEERING

Industrial Engineering roles in semiconductor manufacturing are varies from the IDM and pure play foundry. Roles in pure play foundry are more compared to the IDM. Further breakdown tasks of industrial engineering roles in the big pure play foundry companies and small companies will again shows gap in quantity. Recent update in industrial engineering scopes can be summarized from special issue of the International Journal of Industrial Engineering: Theory, Applications and Practice (IJIETAP) in 2014[22]. The roles from the IJIETAP defines in 24 scopes which include industry ecosystem and supply chains, integration and virtual integration, business models, decision technologies and methodologies, fault diagnosis and predictive maintenance, design for manufacturing(DFM) factory modeling analysis and performance evaluation, capacity and inventory management, planning, scheduling and coordination, Job release and dispatch policies, automated or manual material handling systems (AMHS/MMHS), factory/cell/equipment-level controller design, manufacturing execution systems(MES), advanced process control(APC), decision support systems(DSS), transportations and logistics, human resource management, human factors and ergonomics, productivity improvement, yield enhancement systems and e-diagnosis, equipment engineering systems(EES), automation and remote control, cloud, mobile and wireless applications and agent based intelligent systems. However, this again can be conflicting with other department like Manufacturing systems, production control and manufacturing engineering that have common fundamental education background.

The industrial engineering practices in SilTerra are mainly focus in the department of Industrial and Manufacturing Systems Engineering (IMSE)[23][10]. Based on main focus in key performance activities over two years, this paper will briefly discusses 5 of the 24 scopes from IJIE 2014 specially issues on the roles of Industrial Engineers in the semiconductor Industry regard to starts planning and asses utilization. To cover these areas of responsibility, engineers working in fab industrial and manufacturing systems require a range of skills and experience, including data and systems integration in manufacturing execution systems (MES), equipment interface definition and data extraction methodology, equipment preventive maintenance scheduling, simulation modelling, which commonly using Autosched AP, generic commercial software for reporting, and others commercial software from Applied Materials [12], [24]–[26]

III. FACTORY OPTIMIZATION

Starts planning and assets utilization is a key step in ensuring customer orders are delivered by the committed delivery date. Its help to identify the factory output based on product mix loading. The information needed is equipment capacity that derives from each product or technology. In order to do this the engineer needs to collect data for each step for the product and equipment performance during development stages, production ramping and high volume. This data is collected and verified as needed basis. Typical production pure play foundry has MES that track all data transaction for product to complete each process flow that include during processing in the equipment and also as WIP activity level either waiting or on hold due to verification or quality related issues[10][27][28][29]. This practice makes it easy for the engineer to integrate this information into IMSE systems for data collection purposes.

Fig. 2 shows data collection approach that commonly practices in modern wafer fabrication pure play foundry. The data input are from equipment interface data store detail processing information of the product and the equipment during equipment running state and the MES tracks data for the product and equipment prior processing product. Combining this input the information regards the equipment states, wafer per hour (WPH) and cycle time can be generated for the start planning and maximize the equipment assets for factory optimization purposes. Results of this data collection then is analyzed to isolate know issues from the data collection error and also finalized according to SEMI E10 requirement for the equipment performance report and also WPH for the product mix loaded.

In most fabs, the objective of the manufacturing systems engineering team is to develop and sustain systems that reduce manufacturing approach time and plan WIP execution. The engineering teams also have to be experts in fab computer systems, including:

1. Manufacturing execution systems (MES):
    a. A system that tracks all manufacturing activities, including start and finish processes, travel time, product information and overall process historical and future processing steps.
2. Equipment interfaces:

   a. A system that tracks detailed product activities in the equipment, where information of robot transfer time and real processing time is collected for each processing chamber. This system contains product information for each recipe, which is indexed with the MES to compile reports.
3. Equipment maintenance schedules:
   a. A system for validating equipment availability and ensuring the committed equipment availability meets actual availability.
4. Recipe constraints system:
   a. A home grown software system that tracks and creates recipes for each piece of equipment.
   b. This determines which products are processed on the equipment and is used for planning capacity requirements to manage fab output
5. Advance productivity family (APF) for compiling real time data extracted from the MES.
   a. This system extracts, verifies and reports all product information. It is also the application where industrial and manufacturing systems engineers spend most of their time extracting, compiling and verifying systems data.

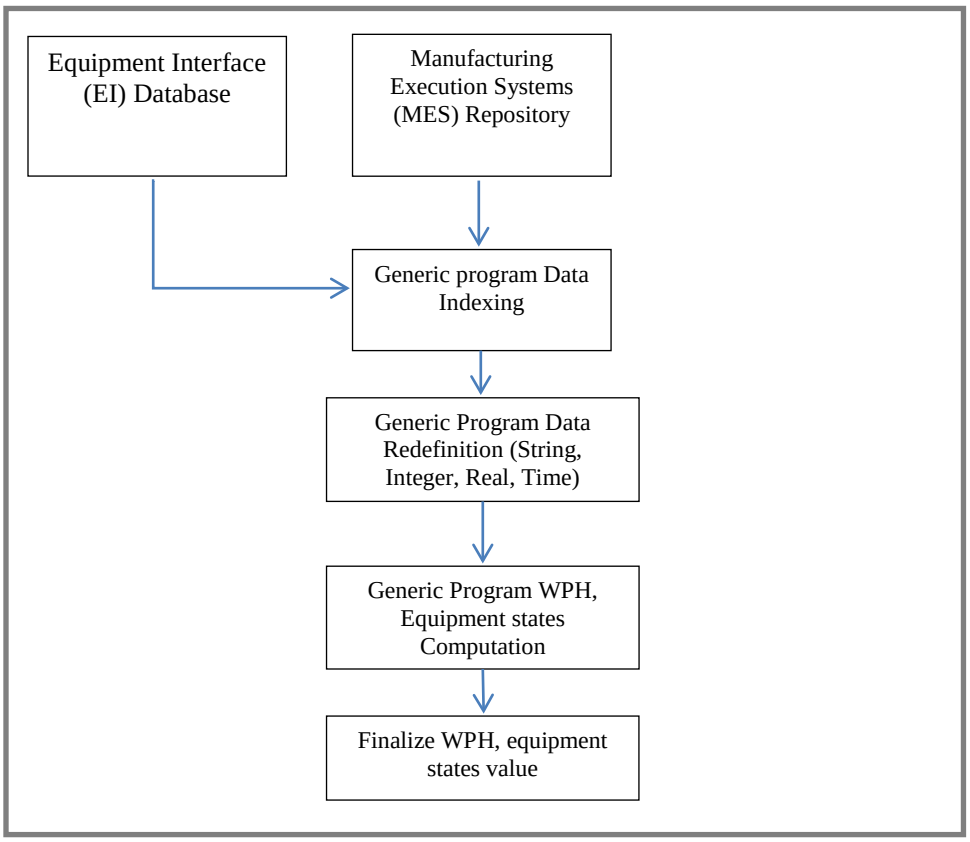


Fig. 2. Generic data extraction diagram

These systems, when integrated with APF, provide a solution that enables engineers to collect, validate and analyze plan and product data. The data are independently validated with MES and other applications to ensure the APF programming logic indexes all the application data properly. Once validation is complete, then the product data are extracted. Modifications to the APF programs, to meet different product requirements, are programmed in UNIX. A high-level architectural overview of the systems integration is presented in Fig. 3.

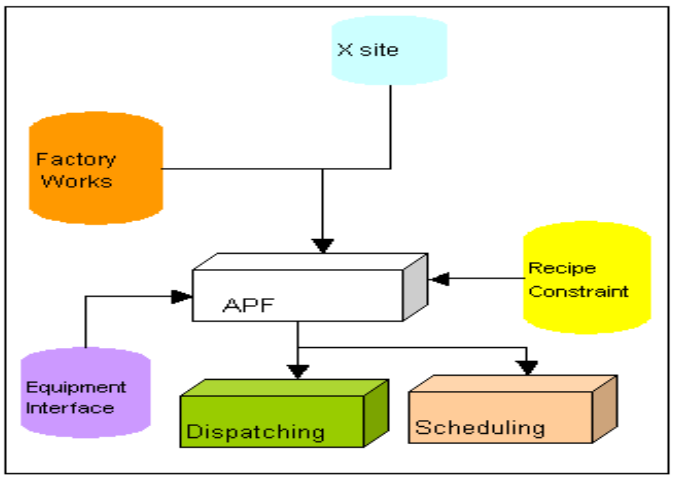
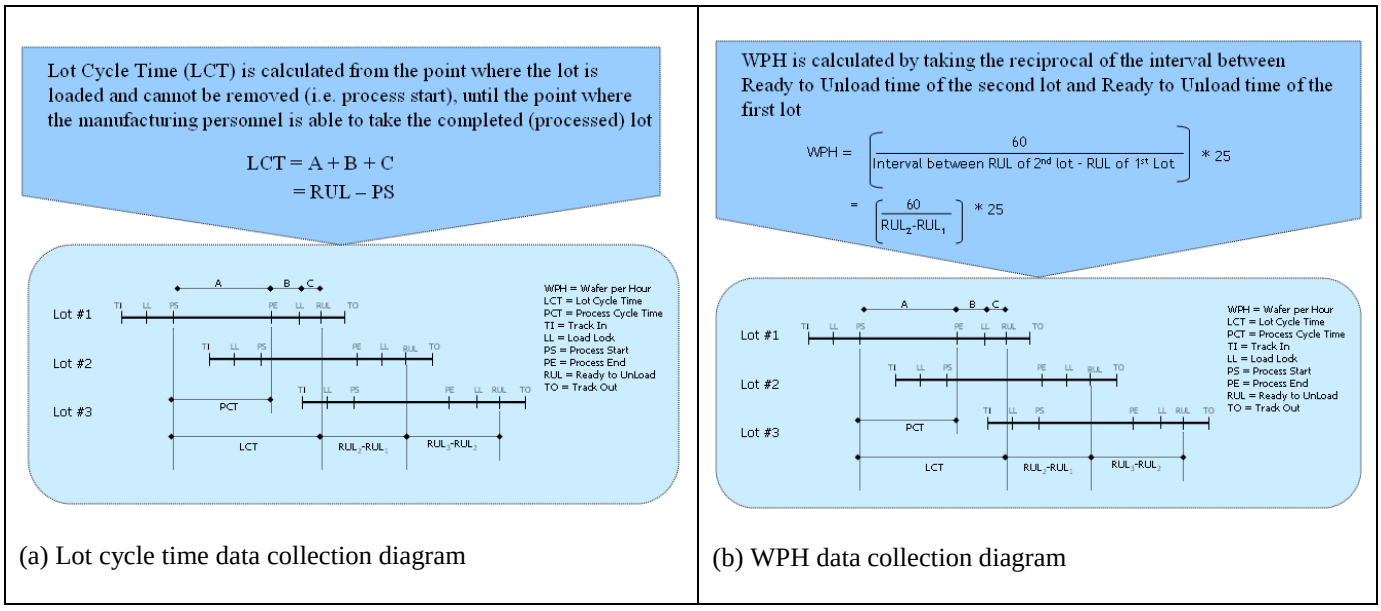


Fig. 3. High-level application architecture of the APF platform for real time data collection

The calculation for the product cycle time and for the WPH is based on APF systems illustrated in Fig. 4. The raw data with details breakdown from equipment key input parameters for WPH calculation, the activity events and event time of equipment are extracted from equipment log. JMP analysis is used to validate and establish WPH and LCT indices.



(a) Lot cycle time data collection diagram

(b) WPH data collection diagram

Fig. 4. (a) Lot cycle time data collection approach and (b) WPH data collection approach.

Table 2 shows example of the results for the equipment performance states that has been collected from the APF platform systems according to the SEMI E10 requirement. The similar format of the results is used for the WPH for each technology used Usually this data are based on more than 10,000 WIP. Data for new technology that is planned for production ramp-up will be based on the qualification data with the engineering team consensus. The results of this data collection will be kept in the IMSE database for the integration in simulation model for capacity validation and also to be used in WIP management with dispatching and scheduling. Figure 4 shows the architecture for the simulation model that utilized data from this stage. Data in Table 2 shows top Bottleneck Equipment (BE), Availability, engineering and downtime

in percentage format. The lowest BE that is available is listed the first in the table. In this example, BE01 is the lowest BE with availability. The productive time is only 65.11% and the standby time is 0.11%. Loss times are in Engineering and non-schedule down time. The capacity determination during this stage will identify bottleneck improvement for the debottleneck activities and planning in the dispatching and scheduling stages.

Table 2: Shows example for the Equipment performance data collection results

Bottleneck Equipment (BE)	Availability (%)		Engineering (%)	Equipment Downtime (%)	
	Productive Time	Standby Time	Engineering Time	Schedule Down Time	Non-Schedule Down Time
BE01	65.11	0.11	14.92	5.87	13.99
BE02	67.32	0.21	11.09	7.92	13.5
BE03	66.93	0.23	10.53	9.58	12.15
BE04	76.79	1.5	7.75	7.52	6.42
BE05	78.69	3.88	8.17	5.21	4.06
BE06	76.78	5.92	6.12	6.63	4.58
BE07	78.29	6.63	4.83	5.88	4.38
BE08	77.88	4.45	6.71	6.612	4.33
BE09	77.35	7.08	2.73	11.04	1.79
BE10	76.19	6.56	3.84	11.26	2.12

Fig. 5 shows a generic simulation modeling configuration that is used to find determine capacity of the factory. To setup the simulation model requires inputs of equipment or tool capability, WIP profile information, tool availability, route information and order information. Many scenario of product mix is analyzed to ensure the factory get the best optimization results.

Once the simulation results complete its run, the data then needed to compute for the capacity of the factory using the formulation in equation (1),

$$\text{Capacity} = \left(\frac{\text{WPH} \times \text{OEE}}{\text{passes}} \right) \times 24 \times \text{period} \times \text{No\_of\_equipment} \quad (1)$$

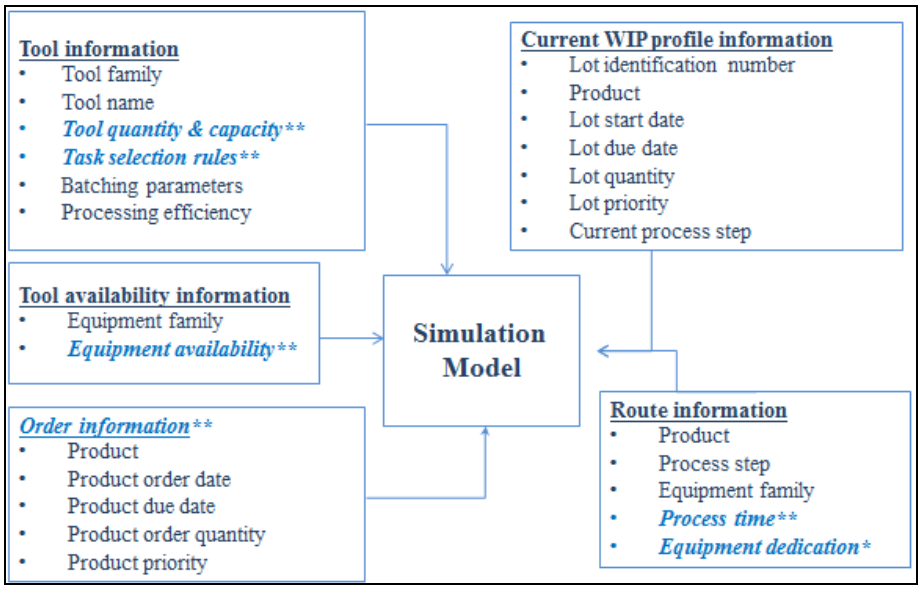


Fig. 5. Simulation model architecture.

Fig. 6 summarized the factory capacity per month based on the technology that is planned to load the factory. The highest loading typically represent the highest utilization [27]. Further analysis on the profit and loss margin related to the loading plans is further discussed with Finance team to decide the optimum mix. Typically high volume translates to lower manufacturing cost and usually gives better profit and loss margin. The product mix trial 2 is the best product mix in term of highest volume which is 25,737. The percentage gain compared to current mix is 14.3%, product mix trial 1 is 11.5% and product mix trial 3 is 26.3%. This heuristic studies help to provide information for better business strategy and kept in the IMSE library for future references. The product information is the process plan, related steps and step cycle time.

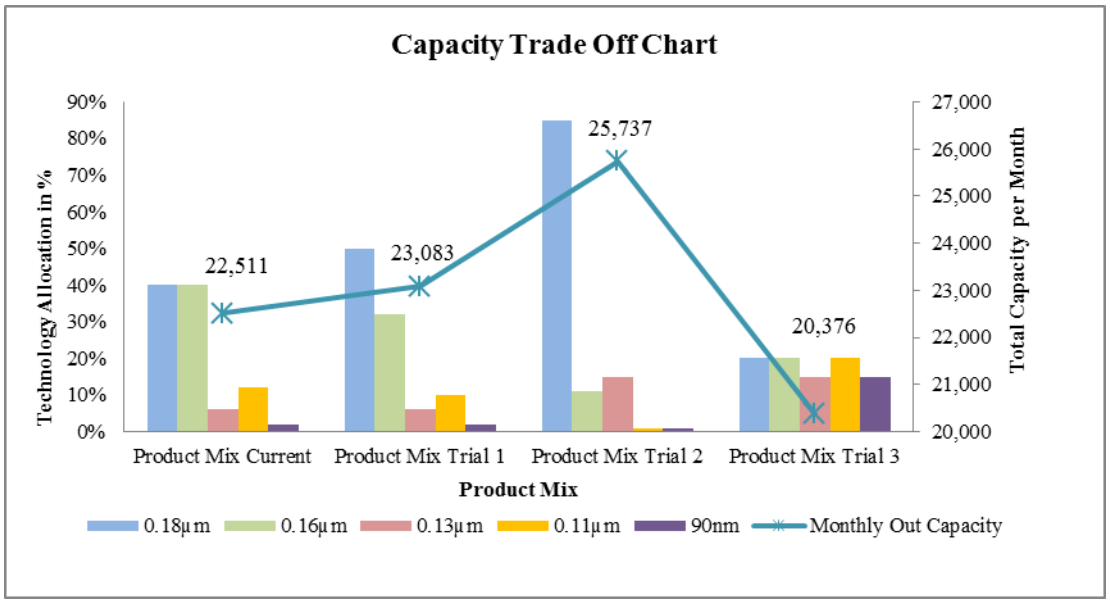


Fig. 6. Capacity Trade Off chart

IV. CONCLUSION

This paper summarizes how Industrial Engineering influences in factory optimization for semiconductor fabrication in the semiconductor foundry, SilTerra Malaysia Sdn. Bhd. The results in this paper is based on IMSE task on starts planning will help to ensure business strategy to gain 14.3% of current product mixed and potentially avoid 10% losses for selecting not optimize mix such as product mix trial 3. As semiconductor business continues to growth through Moore's Law and "More than Moore's Law" this task is becoming more important. Recent news in Malaysia reported that X-fab in Kuching is expanding their capacity [30] and new investment from OSRAM on wafer fab is plant to be constructed in kulim in near term [31]. Because this market continues to expand, industrial engineering will become one of the key careers in engineering. The role requires a multitude of skills and deep knowledge of fabrication processes: cycle time, computer programming and networking, cost of ownership for layout optimization, equipment capability based on existing equipment, benchmarking, and other areas.

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