Yield Improvement of Wafer Edge Die Defocus (EDD) at Via Layers

Arumugam Manikam
Department of Manufacturing Design
Faculty of Manufacturing Engineering,
Universiti Teknikal Malaysia Melaka
76100, Durian Tunggal, Melaka
arumugan_manikam@silterra.com

Dato' Profesor Dr. Abu Bin Abdullah
Department of Manufacturing Design
Faculty of Manufacturing Engineering,
Universiti Teknikal Malaysia Melaka
76100, Durian Tunggal, Melaka
abu@utem.edu.my

Kader Ibrahim Bin Abdul Wahab
Photo Lithography Department
Silterra Malaysia Sdn. Bhd
Kulim Hi-Tech Park
09000 Kulim, Kedah
kader_ibrahim@silterra.com

Abstract

A photolithography process is performed to integrate a semiconductor device on a wafer. A photoresist (is a light-sensitive material used in several industrial processes, such as photolithography and photoengraving to form a patterned coating on a surface) pattern is formed by transferring a layout of a circuit pattern formed on a photo masking onto a photoresist layer on the wafer through an exposure process, and a wafer pattern according to the layout of the designed circuit pattern is formed by a patterning process including an etch process using the photoresist pattern as an etch mask. However, when performing the pattern transfer by processing the exposure shot to the partial field region (edge dies), wafer pattern defects are generated at the edge die field region and poor patterns identify as deform in the Via layers processes, which are the factors of causing yield loss at the edge dies of the wafers. The aim of this proposal is to identify the potential on the lithography aspects of edge die yield loss, with possible solutions and metrics to increase the percentage of yield at wafer edge dies.

Keywords
Lithography, Edge Die, Defocus, Via,Yield