A DMAIC Approach in Improving Wafer Hairline Crack Detection Process at Chip Probe and in Reducing Overall Manufacturing Downtime

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Abstract

Modern microchips are now embedded into everything from cars and washing machines to fighter planes. Today silicon chips are everywhere, driving all forms of digital innovation. If anything, the mercurial rise in market demand for microchips understate the importance of chip making. The silicon wafer is a major component in producing integrated circuits, with sizes that vary in thickness from 275 to 925 µm. A hairline crack is a major defect commonly found in thin wafers in the downstream supply chain of the semiconductor industry. Too high a downtime of 19 hours was incurred with the detection of hairline cracks at the wafer sort process that implemented a Cross Crack Check (CCC) at chip probe (CP). In this case of an outsourced assembly and testing (OSAT) company, a DMAIC (Define-Measure-Analyze-Improve-Control) approach was employed in identifying and addressing the root causes of high CCC flag trigger and validated 4 out of 19 major process contributors to hairline-caused downtime of 4.83% which all resulted in an opportunity revenue loss of $57,000. The study presented corrective solutions in reducing CCC flag trigger from 14 to only 4 wafers and consequently minimizing CCC flag downtime level to 1.53% or from 19 to 3 hours.

Keywords:
Silicone wafer, hairline crack, chip probe, cross crack check flag, DMAIC,

1. Introduction

In the semiconductors industry, the major raw material used to produce integrated circuits is silicon wafer. Si wafer sizes vary from 1 to 12-inch in diameter ("Wafer", 2021), while wafer thickness varies from 275 µm to 925 µm (Bywaferworld, 2019). As the demand for electronic devices (gadgets, smartphones, and TVs) increases, the demand for Si wafers increases as well. As such, the idea of increasing wafer size gives the production of more semiconductor instruments from a single wafer. Furthermore, as these electronic devices require smaller IC, the thinner the wafer is the better. Increase the size and thinner wafers will result in improvements in productivity and effectiveness in the supply of wafers.

Wafer test or wafer sort is one of the major processes in the semiconductors industry. Si wafers are sent for wafer testing prior to die preparation. All individual IC on the surface of the wafers will be subjected to electrical and functional testing. This testing is performed by using an Automatic Test Equipment (ATE) and Prober machine. Wafer sort is also commonly known as circuit or chip probe (CP) ("Wafer testing", 2019). In Wafer Sort, there could be various wafer sizes, 6-, 8- and 12-inch wafers, with wafer thickness it is categorized as standard and thin wafers. Standard wafers are those with 775+/-25 µm thickness measurement, while thin wafers are those with 280+/-20 µm thickness measurement. To reduce the thickness of a standard wafer and convert it to a thin wafer, it would have to go to a process known as grinding. This process will allow stacking and high-density packaging of IC (Pei & Strasbaugh, 2001). In every process, there will always be a corresponding failure mode. Substrate damage is the common failure defect that is induced by grinding. As the diamond grit size increases the crack increases. One of the most difficult to detect on the wafer is the hairline crack, see Figure 1. Several researchers had studied various techniques to detect such defects. One is by using a high repetition rate laser nonlinear ultrasonic system. Eight Si wafers were used to experimentally validate the proposed technique. Results show that by using a high repetition rate laser ultrasonic system, a crack can be detected by 90% (Jang et al, 2020). A team of researchers in Japan utilized the

optical measurement method to analyze wafer surfaces. This technique evaluates the defects by converging a beam on the surface of the wafer. The interference effect of scattered light will manifest the defects on the surface of the wafer (Takahashi et al, 1998). The experiment carried out resulted to be in good agreement with the micrograph by SEM (Scanning Electron Microscope).

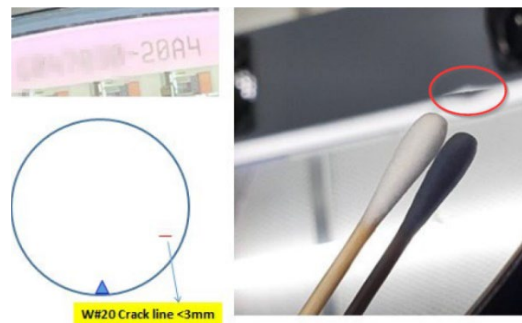

Figure 1. Hairline crack on the backside of the wafer

These grinded wafers (thin) will be received and performs in the Incoming Quality Control (IQC) with the use of the Luxo lamp. However, it would be difficult to detect the hairline size crack defects, hence; a trigger was implemented to detect the hairline crack during electrical testing at the chip probe (CP) process. Table 1 illustrate the overall process flow for wafer sort. The Cross Crack Check (CCC) flag was implemented at Chip Probe (CP) to alert for any potential signature of a wafer having a hairline crack.

Table 1. Wafer Sort Process Flow

No.	Process Step	Remarks
1	W-bank	Wafer Bank
2	IWST	Incoming Wafer System Transfer
3	IQC	Incoming Quality Check
4	CP1	Chip Probe First Insert
5	VM	Visual Mechanical
6	OWST	Outgoing Wafer System Transfer
7	WLPK	Wafer Line Pack

This additional process of CCC flag, however, led to stoppages affecting the overall production cycle time at an average rate of 13.04 % versus an allowable 4.81% downtime for the one year September 2019 to August 2020, resulting in an opportunity loss of US$18,000. This amount was based on the recorded 294 CCC flag wafers that required 1.52 technician hours each resulting in a total downtime of 446.88 hours equivalent to 18 days' setup of 5 wafers each at a US$200 value per wafer.

In this light, the study aimed to improve the incoming quality of wafers received from customers and minimize the overall production setup downtime from 13.04 % to 4.81%. The objectives of the study were: (1) to assess the current process of incoming quality check and sorting of wafers; (2) to identify the root causes of CCC flag downtime from the problematic process established; and (3) to recommend sustainable solutions at the chip probe for hairline crack detection to reduce overall manufacturing downtime.

The study focused on wafer sort processes and factors contributing to the CCC flag. Upstream processes, wafer prep, and WLCSP (Wafer Level Chip Scale Package) process were not be covered as well as the enhancement of the script for the CCC flag.

2. Review of Related Literature

In the semiconductor industry, silicone is the base material in the production of wafers for ICs. It is hard and brittle that conventional grinding is one of the conventional methods in reducing the thickness of Si wafer. Grinding is done by using a coarse diamond abrasive wheel and a fine abrasive wheel. The grit diamond will remove the Si wafer backside material rapidly and at the same time causes damage to it as well. The fine abrasive, on the other hand, will be used to remove the part that is damage on the backside of the Si wafer to ensure the high surface quality of the

wafer (Nichiguchi et al, 1990). The result from the experimental and analytical analysis shows that the damage on Si wafer is mostly can be found on polycrystalline, whereas residual stress will cause the wafer to bend or warp (Chen & Wolf, 2003; Yang et al, 2008; Pei, 1999). It is essential to understand the surface substrate crack or SSC's formation during grinding, as it will identify those contributing processes that cause SSC. By using, statistical method, it was determined that SSC is not stochastic but an anisotropic in distributions.

Various researchers have experimented with several methods and techniques to detect a crack. Takahashi et al (1998) studied the use of scattered light and this method does not only detect cracks but as well as other defects like debris, foreign material, etc. Jang et al (2020) researched the use of a high repetition rate pulse laser which resulted in 90% detection accuracy. The most common inspection method use in the semiconductor industry is Photoluminescence (PL) and Infrared Transmission (IR). Demant et al, (2016) studied the algorithm of PL and IR in improving the accuracy of detection. They do this by inserting an artificial crack image and introduce a pattern recognition approach. The algorithm resulted in 81% for PL images and 98% for IR images. The other promising method is computer vision and electrical tests. Computer vision as described by Israil et al, (2012) uses advanced image processing software to accurately detect and analyze numerous visual inspection problems. Chiou et al, (2011) use a near-infrared (NIR) camera to capture the cracks. This technology can also detect stains, pinholes, etc. In addition, according to Lin et al, (2015), NIR imaging is a non-destructive inspection method. An electrical test on the other hand is a common method for wire bonding interconnection check. Ong & Cheong (2016) investigate Time Domain Reflectometry (TDR) and the results suggested that TDR is an effective electrical test to detect a crack in wire bond stitch.

Downtime is a frequent problem encountered in production or manufacturing industries. According to Al-Aomar et al (2016), downtime will result in an hour lost and while Ashary & Jaqin (2016) believes it causes machine damages. In order to optimize production continually, as mentioned by Windmark et al (2012), it is essential to reduce the frequency and length of downtime. In addition, as concur by Inyiama & Oke (2020) and Larsen et al (2020), understanding the difference between downtime and normal operation will make it easier to identify the degree of downtime pattern or behavior. As agreed by Yew et al, (2019), Inyiam & Oke (2020), and Wiliams (n.d), an automated knowledge base system that can predict failures and downtime visualization can help to bridge the knowledge gap. An improvement of downtime maintenance, for example from 18 to 9 hours, is a great deal because it increases the machines' availability and shortening downtimes.

3. Methodology

Six Sigma DMAIC (Define – Measure – Analyze – Improve – Control) methodology is the common technique used by some researchers to identify and analyze downtime (Milosavljević & Rall, 2005). This is a constructive tool in recognizing processes, which have underlying problems and help to address those problems through a recommendation of improvements and controls. As such, the DMAIC methodology was employed to zero in on the downtime problem of the key process under study with a data-driven investigation and validation of its root causes to come up with sustainable cost-effective improvement solutions in improving crack detection and reducing downtime.

In DMAIC methodology it is essential to perceive the scope of the study, the process selected could be too broad to handle or too small to realize breakthrough improvements. The study might focus on trivial areas and miss out on the vital ones. SIPOC (Supplier – Input – Process – Output – Customer) is a good start to grasp process boundaries. This tool identifies the relationship between supplier, inputs, and the process (Mishra & Sharma, 2014). Another tool is Process Map. These are living documents that provide details of the process to have a clear understanding of the potential causes. This can be accomplished by doing a Gemba walk. As defined by Imai (1997), Gemba is done by walking on the production floor and identify those wasteful processes or activities. Process Capability is a tool wherein the purpose is to investigate if the process can meet the customer CTQ (Critical to Quality) requirements. As per Wu et al (2009), sample data must be collected and the sampling error would have to go for capability assessment. It can be observed that the most used tool in DMAIC methodology is the Pareto chart. Pareto chart, according to Kenett et al (2013), is a simple yet powerful tool, it uses the 80-20 rule for defect analysis, distinguishing "vital view" from "trivial many" and this principle is coined by Joseph M. Juran. Ishikawa or fishbone diagram, according to Inyiama & Oke (2020) will establish cause and effect, one line represents the fish spinal cord and will be extended to the caudal fin. At the end of the caudal fin will then state the 4M1E (Man, Method, Machine, Material, and Environment). ANOVA, Box plot, and Chi-square are the statistical model used to conduct hypothesis testing. As defined by Davis & Mukamal (2006), hypothesis testing determined whether a particular value of interest falls within or beyond the confidence interval, whether those two things are the same or different. Null hypothesis (Ho) state if the testing from two sets of data are the same, while alternate hypothesis state if the testing from two sets of data is the difference.

DMAIC methodology is originally utilized in the manufacturing sector which helps to improve the sigma score. This method has been adopted as well by other sectors such as customer services (Al-Aomar & Almazroui, 2016) sales, health care, software development, marketing, and human resources as it was able to aid these industries to develop a specific process improvement action plan (Snee & Hoerl, 2003). At a present time, with high competition in the market, process improvement is paramount to achieve the increasing demand for customer satisfaction and quality services (Smętkowska & Mrugalska, 2018). Some case studies used the DMAIC technique integrated with lean manufacturing (Jamil et al, 2020). Apart from process improvements, DMAIC eliminates (Gangidi, 2019) or minimized waste, defects, and errors (Patil & Inamdar, 2014; Gangidi, 2019; Gangidi et al, 2011). The application of DMAIC not only provides solutions and profit for the organization but as well as increases customer and employee satisfaction, comfort, and progress (Smętkowska & Mrugalska, 2018; Jamil, 2020).

4. Results and Discussion

A hairline crack is difficult to see through the naked eye. Due to the properties of the passivation coating on the active surface, it will hold the wafer for some time and normally will not give way during processing, not until you flip over the wafer. Figure 2, the wafer is already at the OWST stage, second to the last stage of the wafer sort process. At this stage, the operator will take the wafer from the cassette, flip it over and place it on the canister, facing down. At this point, the undetected hairline crack and with the additional force from the processing of the wafer propagated and finally break the wafer into 2 pieces. The broken wafer can no longer be shipped and need to compensate the customer for the lost revenue.

Figure 2. Wafer crack during the OWST stage.

CCC Flag (Cross Crack Check) was implemented at CP to detect any potential signature of wafers having a hairline crack. However, a broken wafer still can be discovered after the CP stage, furthermore, there is a high downtime induce wherein the majority, as claimed, is invalid. This study will focus on the wafer sort process and factors affecting the CCC flag downtime trigger and improve the CCC detection process at CP in reducing manufacturing downtime.

4.1 Define Phase

This phase started with a Project Charter which provided direction and purpose to the organization and people. Moreover, members from Product Engineer, Process Engineer, Test System Engineer, and Equipment Engineer were identified to be part of the team.

Shown in Figure 3 below is the Wafer sort SIPOC diagram. As defined by Mishra & Sharma (2014), this tool identifies the relationship between supplier, inputs, and the process. Supplier will produce the wafers, and this will be one of the inputs. At input, tester, prober, and temp sensor were also identified. Processes are W-bank, IWST, IQC, CP1, VM, OWST, and WPTC. The expected output is tested wafers. Lastly, to deliver the quality tested wafers to the assembly house and/or customer. This tool provided a better understanding of the major sequence of the key processes.

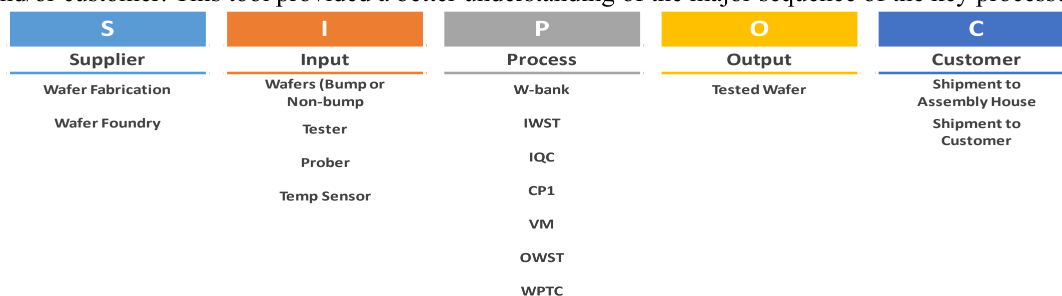

Figure 3. SIPOC Diagram of Wafer Sort

Another tool used was the swim lane, shown in Figure 4, for the wafer sort process detailing the job responsibilities on who does what and showing how delays, mistakes, or cheating were most likely to occur. The process steps were then validated via the Gemba walk that allowed to see what was actually happening compared to what was suspected or brainstormed to the cause(s). As a result, this phase highlighted the 4 process steps as significant contributors to manufacturing downtime.

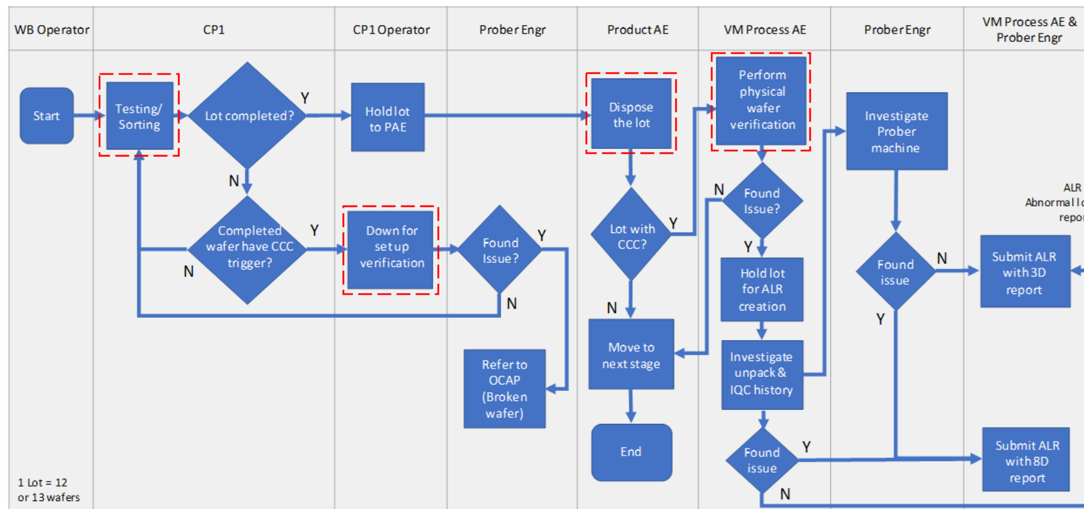

Figure 4. Wafer Sort Process Swim Lane

4.2 Measure Phase

This is the data collection phase in quantifying the problem based on the aforementioned process steps causing the most downtime. The majority of invalid CCC flags came from standard wafers and material-related issues. Downtime data was collected via OEE (Overall Equipment Effectiveness) database and Wafer Slicer.

Based on Figure 5 below, high downtime was observed from periods WW18 to WW31, hence, the root causes of these were investigated in the same period. Furthermore, actual process observations and interviews with the process owner helped determine what changed - the difference between the actual versus the existing procedure. Figure 5 also showed the devices that had a high trigger of CCC flag. By utilizing Pareto's 80/20 rule, Device_01, Device_20, Device_06, Device_04, Device_09, Device_03, and Device_02 comprised the high contributors.

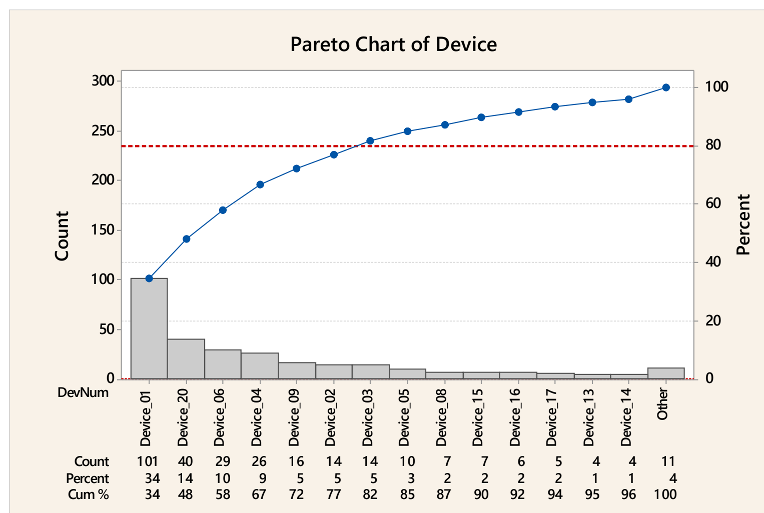

Figure 5. Pareto Chart

The majority of the devices with CCC flags were coming from standard wafers with a wafer thickness of 775+/- 25 um. Moreover, upon wafer inspections, it was noted that most of the CCC flags are considered invalid because of material-related issues. In addition, the rejects bin observed were coming from functional fails as can be discerned from Figure 6.

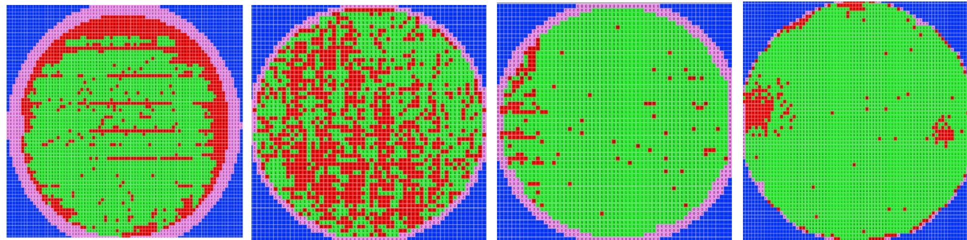

Figure 6. Wafers with functional rejects

Removing the trigger for all standard wafers and material-related issues the focus will be on all thin wafers with a thickness of 280+/-20 um. Table 2 indicates that data is normally distributed with a p-value of 0.316 > 0.05 and appears to be off-target with a CpK of 0.16 < 1.67. By focusing on a specific period, excluding standard wafers with wafer thickness of 775+/- 25 um and wafers with confirmed material related, CCC flag downtime new baseline is 1.53%.

Table 2. Thin Wafers p-value and CpK

p-value	CpK
0.316	0.16

4.3 Analyze Phase

The third phase aimed to identify probable root causes and determine the real root causes and/or its major source contributors. Accordingly based on the swim lane and from the data/information collected, four (4) process steps were found to be significantly associated with CCC flag downtime, namely: testing/sorting; down for setup verification; disposing of the lot; and performing physical wafer verification.

Consequently, this information helped outline the conduct of the Ishikawa or fishbone diagram shown in Figure 7. In summary, one (1) possible cause each was identified for Machine, Material, Man, and Measure and two (2) probable causes were attributed to Method, thereby, giving a total of 6 possible root causes.

With reference to define phase, the four (4) process steps were associated with CCC flag downtime which was based on the data obtained from the measure phase, and together yielded the real root causes. Root causes were validated using hypothesis testing and the p-value approach. As result, 3 out of 6 potential root causes were found to be valid.

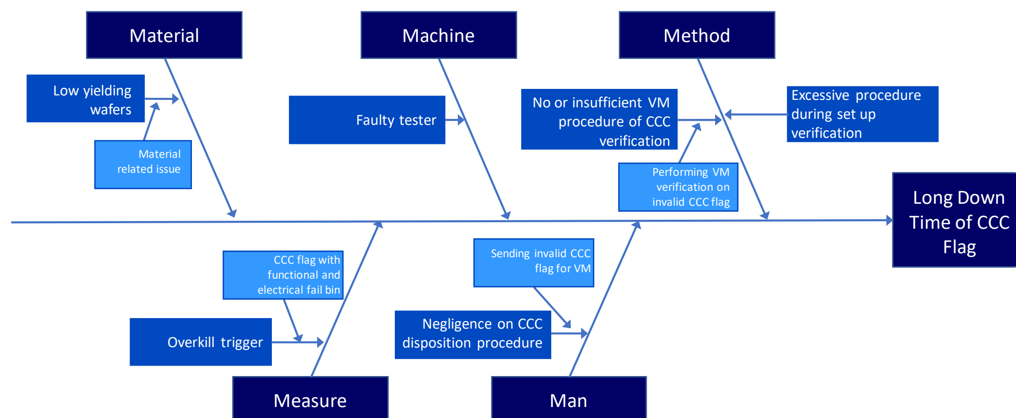

Figure 7. Ishikawa diagram

Table 3 is the validation results from 62 sample size. Applying 1 sample t-test and 2 sample t-test, several factors were found to have a significant association that affects the overall downtime of the CCC flag. 3 out of 6 potential causes were found to be valid, wherein the p-value is < 0.05. First, overkill bin trigger in which the script triggered fail on all bins including functional test. Second, Negligence in the procedure, sending invalid triggers such as low-yielding wafers for visual machine inspections. Lastly, no, or insufficient procedure in assessing the CCC flag.

Table 3. Validation Table

Process Function	Input	Practical Theory		Validation Method		With Significant Difference?	P-Value
		Process Failure Mode	Effect of Failure Mode	What to Test	Stat Test		
Testing/ Sorting	Wafer yield	Low yielding wafers due to material related issues	Invalid flagging of various test check items	Average CCC downtime	2 Sample t-Test	N	0.671
	Test bin results	Overkill bin trigger.				Y	0.004
Down for setup verification	Setup verification SOP	Excessive procedure. The scope of verification go farther than necessary	Unnecessary downtime	Average time spent in attending to setup with CCC flag	1 Sample t-Test	N	1.000
	Tester data log	Faulty tester causing low yield		Average CCC downtime	2 Sample t-Test	N	0.671
Dispose of the lot	Disposition SOP	Negligence on the procedure. Sending invalid trigger for VM inspections.	Wrong disposition of the lot	Average CCC downtime	2 Sample t-Test	Y	0.000
Physical wafer verification	Verification SOP	No or insufficient procedure in assessing CCC flag	Unnecessary downtime	Average CCC downtime	2 Sample t-Test	Y	0.000

4.4 Improve Phase

In this phase, a team was assembled from the cross-functional departments and did brainstorming and one-point lesson sharing of best practices. Based on brainstormed ideas and collected information on validated root causes, four (4) improvement solutions were generated, to wit:

1. Enhance the script to trigger specific h/s bin related to CCC.
2. Stop the machine, if CCC is encountered for 3 consecutive wafers, for confirmation.
3. Change the procedure to send only wafer for VM inspections after 3 consecutive triggers.
4. Apply gating of lots with wafers triggered CCC failure before the PAT process.

During the test program investigation from past confirmed cases of hairline crack. The test parameters will fail on contact test, open-short test, leakage test, and supply test, hence, eliminating the functional parameter test and enhancing the script to triggered specific h/sbin related to CCC will address the overkill bin trigger.

To resolve the negligence on the procedure, such as sending an invalid trigger, 2 corrective actions were formulated. First, instead of prompting the tester for setup confirmation on every CCC flag, it was concurred to execute the setup confirmation on every 3 consecutive CCC flags. The purpose of setup confirmation is to determine if the CCC flag is not induced by in-line processes, such as screw falling on chuck table thus during test the screw is scratching the surface of the wafer or prober arm scraping the wafer surface. Such circumstances will not only damage 1 wafer but

the succeeding wafers as well. This is then deemed as true downtime due to an in-line process issue. Second, generated a procedure to send only wafer for VM inspections for 3 consecutive triggers.

To overcome an insufficient procedure in assessing the CCC flag, a gate was placed to block the movements of lots with CCC triggered to the next process. Figure 8 is an image of the PAT (Parametric Average Test) process blocking CCC wafers until VM inspection is successfully executed.

```
Wafers failing cross crack fail : 04
Wafers pending VM scan          : 04
PAT will be blocked until Cross crack fail wafers are scanned.
RemotePAT_start aborted:Cross crack check
LRMS4<st3>3>
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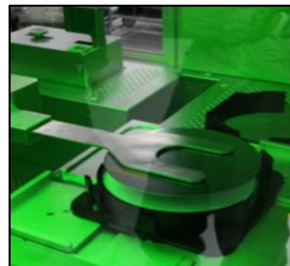
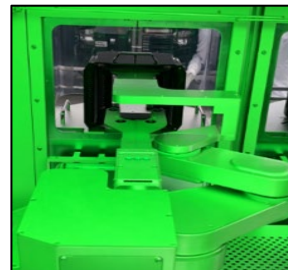
Figure 8. PAT process script

Aside from addressing the root causes, investing in auto transfer and inspection machines is a good decision to make. This machine was allocated at IQC and OWST, thus, eliminating manual handling and inspections of wafers. Figure 9 is the auto-transfer machine that can shift a wafer from canister to cassette during IQC and vice versa can shift a wafer from cassette to canister during OWST.



Wafer on canister



Wafer in cassette

Figure 9. Auto wafer transfer from the canister to cassette vice versa

Figure 10 is the auto inspection capability of the machine. The machine is able to detect any surface defect that can be found on the wafer.

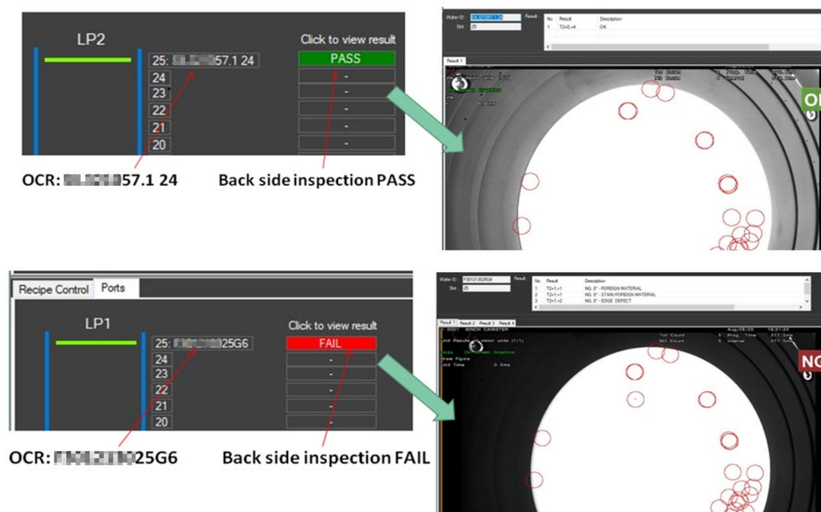


Figure 10. Auto inspections – Pass & Fail

Removing of standard wafers, material related, and focusing on specific h/sbin show a significant drop in wafers triggering the CCC flag. Moreover, setting of 3 consecutive wafers prior to setup conformation, updating disposition comment, and CCC failure to send for VM inspection before PAT process show a significant drop in downtime. Based on Figure 11, CCC flag trigger decreases from 14 wafers to 4 wafers on average while downtime decreases from 19

hours to 3 hours on average. The introduction of auto transfers and inspection machine help to eliminate the manual +handling and inspection of wafers, hence, reducing the risk of operator breaking the wafer if there is an inconspicuous hairline crack.

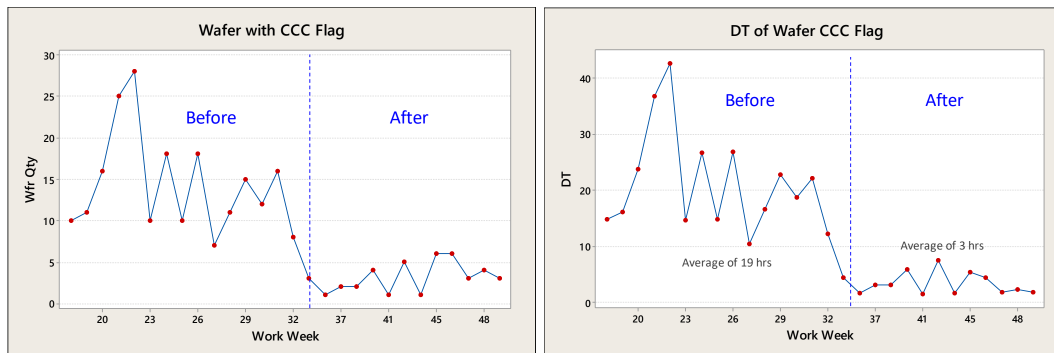


Figure 11. Implementation Results

The above results were the team's assessment of the effectiveness of the identified solutions.

4.5 Control Phase

Table 4 represents the Process Control Plan for the CCC flag 30% straight line of identified h/sbin failure will prompt a message at every end of the wafer, technician will validate if this flag is a 3rd prompt. If confirmed 3rd CCC flag, a technician will validate the setup and PAE (Product AE) will dispose of the lot for VM inspection. PPR will conform to any physical crack on the failure area of the affected wafer. As compared to the old practice, this new procedure will reduce the unnecessary setup downtime. Apart from the generation of the Process Control Plan, Cross Crack work instruction was also created and documented. This is essential as it provides a sequence of activities in a process and defines who is responsible for those activities.

Table 4. CCC Flag Process Control Plan

Process Steps	What Controlled?	Input/ Output	Spec. Limits	Measurement Method	Control Method		Sample Size	Frequency	Who/ What	Corrective Action	SOP
					Type	Details					
Testing /Sorting	Sbin & Hbin	Output	30% straight line	In-site system count	Alert Message	Every wafer end	Affected wafer	Daily	Tech	Validate if 3rd trigger	A-XX-MF-090317-AP13 & WS Dispo Guide
Dispose the lot	CCC Flag	Output	3 consecutive CCC wafers	Wafer map	Wafer Slicer	Every wafer end	3		Tech	Validate the setup	
									PAE	Hold and send wafer for VM inspection	
Perform physical wafer verification	Wafer being inspected	Output	3 wafer with CCC flag	Visual checking	Inspection	Affected wafer and area	Affected area of the wafer		PPR	Conform physical crack on failure area of affected wafers	

The last phase of the DMAIC process formulated the above improvement plans in view of sustaining the desired gains by documenting and standardizing enhanced procedural steps and by disseminating them with known metrics and targets for control and review purposes to be contained in an updated Control Plan and Work Instructions.

5. Conclusion

DMAIC methodology was able to dissect the problem of hairline cracks, brought to light the root causes, improve the process steps accordingly, and integrate them in the wafer hairline crack detection process at the chip probe, resulting in reduced manufacturing downtime.

The high occurrence of broken wafers at the wafer sort process resulted in not meeting shipping schedules, a critical-to-quality (CTQ) concern to the customer, experiencing delays in shipment. By utilizing DMAIC methodology the 3 objectives of the study were systematically investigated.

Objective 1, to assess the current process of incoming quality check and sorting of wafers define phase was used. 4 out of 19 process steps were determined as a contributor of downtime. The second objective uses the measure and analyze phase to identify the root causes of CCC flag downtime from the problematic process established from objective 1. CCC flags from standard wafers and material-related issues are regarded as invalid and excluded during the deliberation of normal distribution, process capability, and target baseline. 6 potential root causes were identified and from a 62 sample size, these potential root causes were validated using 1 sample t-test and 2 sample t-test. As a result, 3 out of 6 potential root causes were found to be valid. The last and third objective applies to improve and control phase of the DMAIC process, to recommend improvement solutions on the identified root causes established from objective 2. The proposed improvement actions were documented and updated accordingly to make certain that it won't revert to old ways.

6. Recommendation

DMAIC is a useful tool for process improvements as it sustenance a structured fashion of improving the process. Moreover, it gives an essential understanding of customer needs and expectations, Voice of Customer (VOC), and empathizing process performance over time, Voice of Process (VOP). Further research may utilize FMEA to assess the existing process. In addition, to explore as well standard wafers and other possible equivalents h/sbin failure of a hairline crack. This may include upstream processes to eliminate the probable causes of a hairline crack and emerging technology can also be utilized to improve operational effectiveness.

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