Accurate modeling and simulation of the thermal effects on the mechanical properties of Silicon, Germanium, and Silicon-Germanium materials used in nanotransistors and solar cells

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Abstract

The aim of this paper is to develop accurate models to take into account the effects of the fabrication temperatures on the elastic constants of Silicon, germanium, and Silicon-Germanium thin films used as performance boosters in the new generation of nano pMOS and nMOS transistors and solar cells. We are calculating the elastic constants of Silicon-Germanium (Si(1-x)Ge(x)) using a linear extrapolation based on the Germanium mole fractions x and the elastic constants of Silicon and Germanium materials. And, to calculate accurately the temperature dependent elastic constants of Silicon and Germanium, we are using Taylor's expansion around room temperature with polynomials of degree two.
We found an excellent agreement between the calculated temperature dependent elastic constants and the experimental data. The values of the calculated elastic constants of Si(1-x)Ge(x)) films have been used to calculate accurately the resulting intrinsic and extrinsic stresses in 14 nm nano pMOS transistors developed by Intel in 2014. We found out that the values obtained for theses intrinsic and extrinsic stresses are in excellent agreement with the experimental data found in literature. The obtained simulation results in three dimensions will be presented and analyzed for various temperatures.

Keywords
Thermal effects, elastic constants, Silicon-Germanium, stress, strained nanotransistor

1. Introduction

The electrical performances of micro scale CMOS transistors have been continuously improved by the traditional geometric scaling following Moore's law. The gate oxide thickness scaling, junction scaling, and the common collector voltage scaling were the main methods used in the traditional geometric scaling. The year 2000 marked the end of this traditional geometric scaling era that lasts about 50 years. The geometric scaling did help increase the performances of micro scale CMOS transistors between the year of their invention (1947) and 2000. But, the geometric scaling alone could not help increase the performances of nano scale CMOS transistors that were born in the end of 1999. In the year 2000, the CMOS research team at Intel company have faced serious challenges when they have used the traditional geometric scaling to fabricate the nano scale 90nm CMOS transistor (Ghani, 2009). The top challenges for this nano scale 90nm CMOS were: the parasitic resistance, the gate leakage, and the mobility degradation due to channel ionized impurity scattering (Ghani, 2009).

In its innovations in 2000, Intel has used a tensile stress coming from Silicon-Nitride capping layer to enhance the mobility of nano nMOS transistors by more than 30% (Ghani, 2009). For nano pMOS transistors, Intel has used a compressed Silicon-Germanium (Si(1-x)Ge(x)) thin films in source and drain to introduce intentionally a compressive uniaxial extrinsic stress σ in the channel (see Figure 1). Here x represents the Germanium mole fraction. This compressive stress σ is used to enhance dramatically the mobility of holes by more than 50% (JianLi et al., 2014; Chui et al., 2007; Ghani et al., 2003). It has been shown in (Moroz et al., 2006) that the application of this compressive stress σ has enhanced the mobility of holes in nano pMOSFETs by 200%.

This extrinsic stress σ is due mainly to an intrinsic (i.e. initial) stress σ_0 that is generated in Si(1-x)Ge(x) thin films after their growth at high temperatures. This intrinsic stress σ_0 is the sum of the initial stress σ_0^{mm} that is due to material mismatch and the intrinsic thermal stress $\sigma_0^{tm}(T)$ that is due to thermal mismatch between Si(1-x)Ge(x) thin films and Silicon substrate. Here T represents the fabrication temperature of the Si(1-x)Ge(x) thin films. From mechanical point of view, the initial thermal stress $\sigma_0^{tm}(T)$ depends strongly on the elastic constants C11, C12, and C14 of the Si(1-x)Ge(x) thin films.

The aim of this paper is to develop an accurate mathematical model to calculate accurately the elastic constants C11, C12, and C44 of Si(1-x)Ge(x) thin films from the elastic constants of Silicon and Germanium using Vegard's law. In the most commercial device simulation software or papers found in literature, these elastic constants are considered constants. It means they are considered independent on temperature and any other parameters as doping or crystal orientation. Physically, these elastic constants depend strongly on the temperature. The first originality of this paper is that the proposed model takes into account the effects of the fabrication temperatures on the elastic constants C11, C12, and C44 of Si(1-x)Ge(x) thin films. The second originality is the application of this model to calculate accurately the thermal induced intrinsic stress $\sigma_0^{tm}(T)$ in Si(1-x)Ge(x) thin films and the resulting extrinsic stress σ in the whole structure of a 14 nm nano pMOS transistor developed by Intel in 2013. This sample structure is shown in Figure 2. In literature, we could not find any theoretical model that includes the effects of the fabrication temperatures on the elastic constants C11, C12, and C44 of Si(1-x)Ge(x) thin films to calculate the thermal induced intrinsic stress $\sigma_0^{tm}(T)$ and the resulting extrinsic stress σ.

This paper is organized as follows. Section 2 presents the mathematical relation between stress and carriers mobility and explains how stress enhances the speed of nanotransistors. Section 3 outlines the proposed models for the temperature dependent elastic constants C11, and C12 of Silicon-Germanium (SiGe) thin films. Section 4 shows the calculated values of C11 and C12 for different temperatures and compares them with the values obtained from measurements. This section also shows how the calculated values of C11 and C12 are used to calculate the thermal induced intrinsic and extrinsic stresses. The calculated values of the extrinsic stress are compared and validated with the experimental values from literature. The conclusion is drawn in section 5.

2. How stress enhances the performances of nanotransistors and solar cells

The electrical performances of microscale or nanoscale transistors depend strongly on the velocity (v) of the electrons and holes that are flowing in these transistors. Therefore, to increase the performances of transistors we should increase the carrier's velocity v. Mathematically, the velocity v is related to the carrier's mobility μ as follows:

$$v = \mu E \,, \tag{1}$$

where E represents the applied electric field. And, the carrier's mobility is related to the fabrication induced extrinsic stress tensor $\sigma = (\sigma^{xx}, \sigma^{yy}, \sigma^{zz}, \sigma^{xy}, \sigma^{yz}, \sigma^{zx})$ by the following Equation given in (Kumar et al., 2012):

$$\mu = \frac{1}{\mu_0}((A1 - A2)/(1 + \exp((\sigma_{eff} - \sigma_e)/t)) + A2), \quad (2)$$

where σ_{eff} represents the effective extrinsic stress given by the relation: $\sigma_{eff} = \sum_{i=1}^{3} \alpha_i \sigma_{ii} + \sum_{J \geq i}^{3} \sigma_{ii}\sigma_{jj}$. The values of the parameters $\mu_0, A1, A2, \sigma_e, t, \alpha_i$ are given in (Kumar et al., 2012). Here $\sigma_{11} = \sigma^{xx}, \sigma_{22} = \sigma^{yy}, \sigma_{33} = \sigma^{zz}$ represent the normal components of the extrinsic stress σ . The shear stress components $\sigma^{xy}, \sigma^{yz}, \sigma^{xz}$ were ignored in the stress dependent mobility model in Equation (2). From (Kumar et al., 2012), the terms $A1 - A2$ and t in Equation (2) are positive for holes in <110> direction. Then, the mobility μ of holes will increase with decreasing stress. This is way we are using compressive stress (negative stress) to enhance the mobility of holes in pMOS nanotransistors in <110> direction.

From Equation (2), if we use a large compressive stress (negative stress σ) we will increase the mobility of holes. And, if we increase the mobility of holes, we will increase the velocity of holes and, then, the electrical performances of nano pMOS transistors. Stress will also reduce the band gap energy since the conduction band and the valance band will be split up under the effect of stress. And, if we reduce the band gap, we will enhance the optical efficiency of solar cells. In this paper, we will focus only on the impact of stress on nanotransistors.

On the other hand, the compressive stress σ is generated from the thermal induced intrinsic stress $\sigma_0^{tm}(T)$ that builds in Si(1-x)Ge(x) thin films during fabrication. We use Hooke's law to find the relation between $\sigma_0^{tm}(T)$ and σ as follows:

$$\sigma = D\varepsilon - \sigma_0 + \sigma_{00}. \quad (3)$$

Here σ_{00} is taken to be zero for simplicity. And, σ_0 is the thermal induced intrinsic stress which is equal to $\sigma_0^{tm}(T)$ in Si(1-x)Ge(x) films and 0 elsewhere. The terms D and ε represent the stiffness matrix and the strain tensor respectively. A detailed description on how to use finite volume method and the right boundary conditions to solve numerically the elastic model (3) to calculate σ in 3D is given in (El Boukili, 2010). In the same way, we use Hooke's law to calculate the thermal induced intrinsic stress $\sigma_0^{tm}(T)$ in terms of thermal induced intrinsic strain $\varepsilon_0^{tm}(T)$ as follows:

$$\sigma_0^{tm}(T) = D.\varepsilon_0^{tm}(T). \quad (4)$$

To calculate accurately the extrinsic stress σ in Equation (3), we need to calculate accurately the intrinsic stress $\sigma_0^{tm}(T)$ in Equation (4). And, to calculate accurately $\sigma_0^{tm}(T)$ we are going to include the effects of the fabrication temperatures and Germanium mole fractions on the stiffness matrix D which depends on the elastic constants C11, C12, and C14 of Si(1-x)Ge(x) films.

3. Proposed models for elastic constants of Silicon-Germanium thin films

Under the effects of temperature, the stiffness matrix D in Si(1-x)Ge(x) films is given by:

$$D = \begin{bmatrix} c11(T) & c12(T) & c12(T) & 0 & 0 & 0 \\ c12(T) & c11(T) & c12(T) & 0 & 0 & 0 \\ c12(T) & c12(T) & c11(T) & 0 & 0 & 0 \\ 0 & 0 & 0 & c44(T) & 0 & 0 \\ 0 & 0 & 0 & 0 & c44(T) & 0 \\ 0 & 0 & 0 & 0 & 0 & c44(T) \end{bmatrix} = (c_{ij}^{Si(1-x)Ge(x)}(T)) .$$

To calculate accurately the temperature dependent elastic constants $c_{ij}^{Si(1-x)Ge(x)}(T)$ of Si(1-x)Ge(x) films, we are proposing the following new, original and accurate model:

$$C_{ij}^{Si(1-x)Ge(x)}(T) = (1-x)C_{ij}^{Si}(T) + xC_{ij}^{Ge}(T). \quad (5)$$

Here, $c_{ij}^{Si}(T)$ and $c_{ij}^{Ge}(T)$ represent the elastic constants of Silicon (Si) and Germanium (Ge) respectively. And, to calculate accurately the temperature dependent elastic constants $c_{ij}^{Si}(T)$ and $c_{ij}^{Ge}(T)$, we are proposing and using the following models based on Taylor's expansion around room temperature T0:

$$C^{Si}_{ij}(T) = C_{ij}^{Si,0}\left[1 + a^{Si}_{ij}(T-T0) + b_{ij}^{Si}(T-T0)^2\right], \quad (6)$$

$$C^{Ge}_{ij}(T) = C_{ij}^{Ge,0}\left[1 + a^{Ge}_{ij}(T-T0) + b_{ij}^{Ge}(T-T0)^2\right]. \quad (7)$$

Where $C_{ij}^{Si,0}$ and $C_{ij}^{Ge,0}$ represent the elastic constants of Silicon and Germanium at room temperature T0. And, $a_{ij}^{Si}, b_{ij}^{Si}, a_{ij}^{Ge}, b_{ij}^{Ge}$ represent the first-order and the second order temperature coefficients of the elastic constants of Silicon and Germanium respectively. Here, the index i is equal to 1 and j is equal to 1 or 2. C44 is not needed to calculate the initial stress $\sigma_0^{tm}(T)$ since we have ignored the shear stresses components of $\sigma_0^{tm}(T)$.

The values of the Silicon constants $C_{ij}^{Si,0}$, a_{ij}^{Si}, b_{ij}^{Si} are extracted from the measurements values given in (Elding et al., 2015, Antti et al., 2014, Matthew et al., 2010, Bourgeois et al. 1997). The values given in (Antti et al., 2014) are also depending on doping concentrations. In this work, we are taking average values with respect to doping. The results we get for the elastic constants of Silicon ($C_{ij}^{Si}(T)$) are given in the Table 1 bellow. The model in Equation (7) for Germanium is new, original and accurate. We should note that not that much theoretical or experimental work has been done in the literature for Germanium material. We are using the nonlinear least squares method to fit the model in Equation (7) with the measurements from (Madelug et al., 2001) to calculate the values of the constants $C_{ij}^{Ge,0}$, a_{ij}^{Ge}, b_{ij}^{Ge}. The results for $C_{ij}^{Ge}(T)$ are given in Table 1. The values we get for $C_{ij}^{Si(1-x)Ge(x)}(T)$ using the model in Equation (5) are given in Table 1 as well.

4. Numerical results, validations, and analysis

4.1 Validation of the proposed models for elastic constants with measurements

The following Table 1 summarizes the calculated values, in GPa, of the temperature dependent elastic constants of Si, Ge, and Si(1-x)Ge(x) using the models we proposed in Equations (5),(6), and (7) where x=35% and the temperature T is ranging from 25°C to 882°C. The values for the elastic constants of Silicon are in good agreement with the measurements from (Antti et al., 2014). The values for the elastic constants of Germanium are in good agreement with the measurements from (Madelug et al., 2001). And those for Si(0.65)Ge(0.35) are in good agreement with the measurements from (Siqing et al. 1992).

Table 1: C11(T) and C12(T) of Si, Ge, and Si(0.65)Ge(0.35) in GPa.

T in °C	Ge: C11;C12	Si(0.65)Ge(0.35): C11;C12	Si: C11;C12
25	124; 41.3	115.08;55.70	164.14;63.46
100	123.36; 40.97	149.36;55.29	163.36;63.00
300	121.18;40.09	146.72;54.10	160.47;61.65
500	118.27;39.17	143.20;52.86	156.62;60.23
700	114.64;38.73	138.80;51.57	151.81;58.77
800	112.55;37.73	136.27;50.91	149.04;58.01
882	110.71;37.32	134.03;50.36	146.60;57.38

We can see from the Table 1 that the values of the elastic constants C11(T) and C12(T) are decreasing with increasing temperature. This will have a significant effect on the mechanical and electrical properties of these materials and also on the performances of the nano pMOS or nMOS devices using these materials. The values of the elastic constants of Si(0.65)Ge(0.35) in Table 1 are between those of Germanium and Silicon which is in excellent agreement with the theory and experiments (Siqing et al., 1992). As far as we know, the models we have proposed in Equations (5) and (7) for Germanium and Si(1-x)Ge(x) are new and original. No theoretical model has been found in literature for the temperature dependent elastic constants of Germanium and Si(1-x)Ge(x). We believe that not many work has been done for Germanium and Si(1-x)Ge(x) because Silicon is the most employed material in semiconductor industry. Integrated circuits, solar cells, and Micro electro mechanical systems (MEMS) extensively use Silicon and not Germanium or Si(1-x)Ge(x).

4.2 Validation of the elastic constant's models using simulation results of the extrinsic stress

In this section, we are going to validate and apply the models we have developed in the Equations (5), (6), and (7) to calculate accurately the thermal initial stress $\sigma_0^{tm}(T)$ using the Equations (4). And, we are going to use this thermal initial stress $\sigma_0^{tm}(T)$ to calculate numerically the resulting extrinsic stress σ using the Equation (3) in the whole nano pMOS transistor shown in Figure 2. This nano pMOS belongs to the 14 nm technology node developed by Intel in 2014. The gate length of this nano pMOS is 23 nm. Its source and drain are made up of Si(0.65)Ge(0.35) thin films.

Figure 3 shows the extrinsic stress distribution along channel (σ^{xx}) when the elastic constants of Si(0.65)Ge(0.35) thin films are independent of temperature. Figure 4 shows the stress distribution along channel when the elastic constants depend on temperature T when T=500°C. Figure 5 shows the stress distribution along channel for

T=882°C. From Figure 3, the magnitude of the average value of the stress along channel is 4955e+5 Pa and from Figure 4 the magnitude of the average value of the stress along channel is 4330e+5 Pa. Then, the absolute value of the difference is 625e+5 Pa. And, this is a huge difference. We could then say that the values of stress are overestimated when the effects of temperatures are not included in the elastic constants. We can then conclude that to get accurate and correct values of the stress in the channel of a nano pMOS or nMOS transistor, we should take into account the effects of the fabrication temperatures on the elastic constants. As far as we know, no work has been done in the past to investigate this crucial issue. From Figures 4 and 5 we could note that the magnitude of the stress along the channel is increasing with increasing temperature. The obtained values for the extrinsic stress along channel shown in Figures 4 and 5 are qualitatively in good agreement with the measurements given in (Peng et al., 2006).

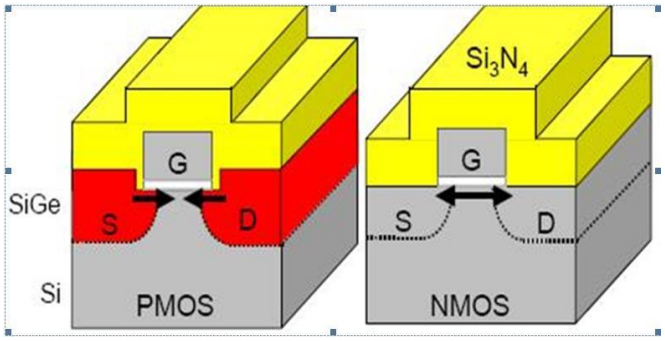

Figure 1: Intel technology for PMOS and NMOS.

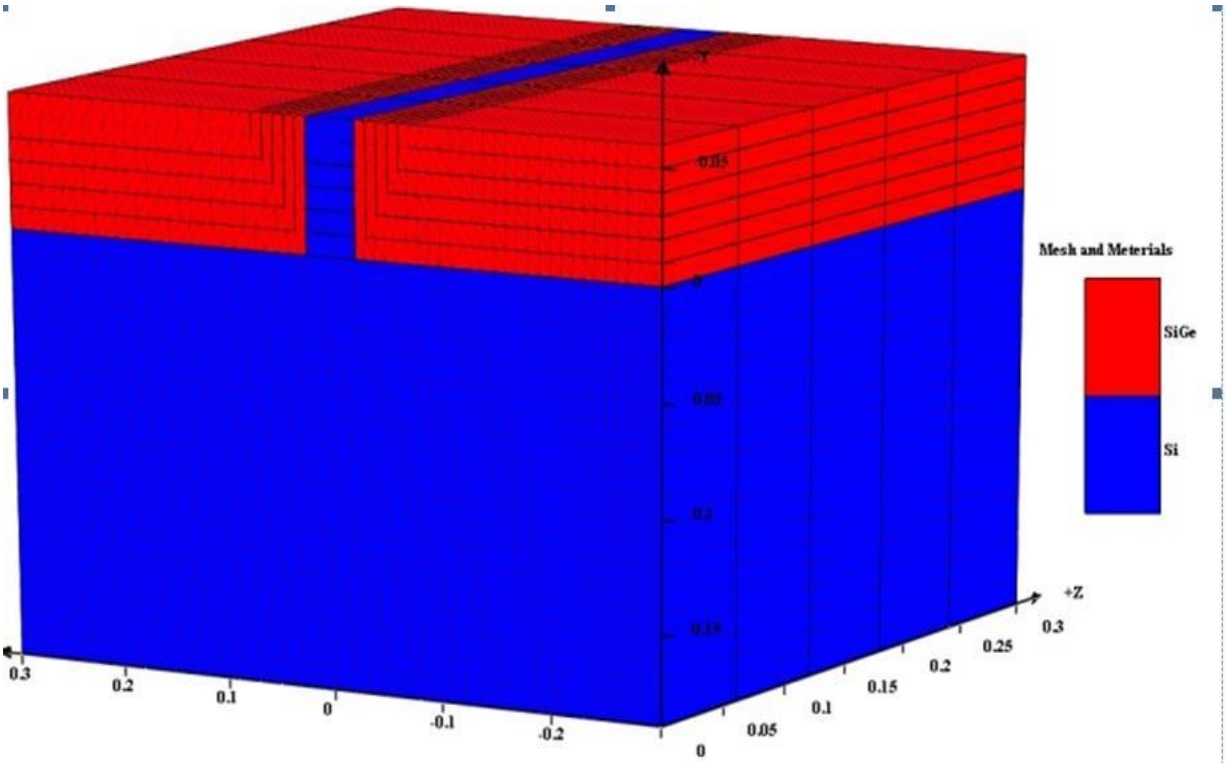

Figure 2: Sample PMOS structure.

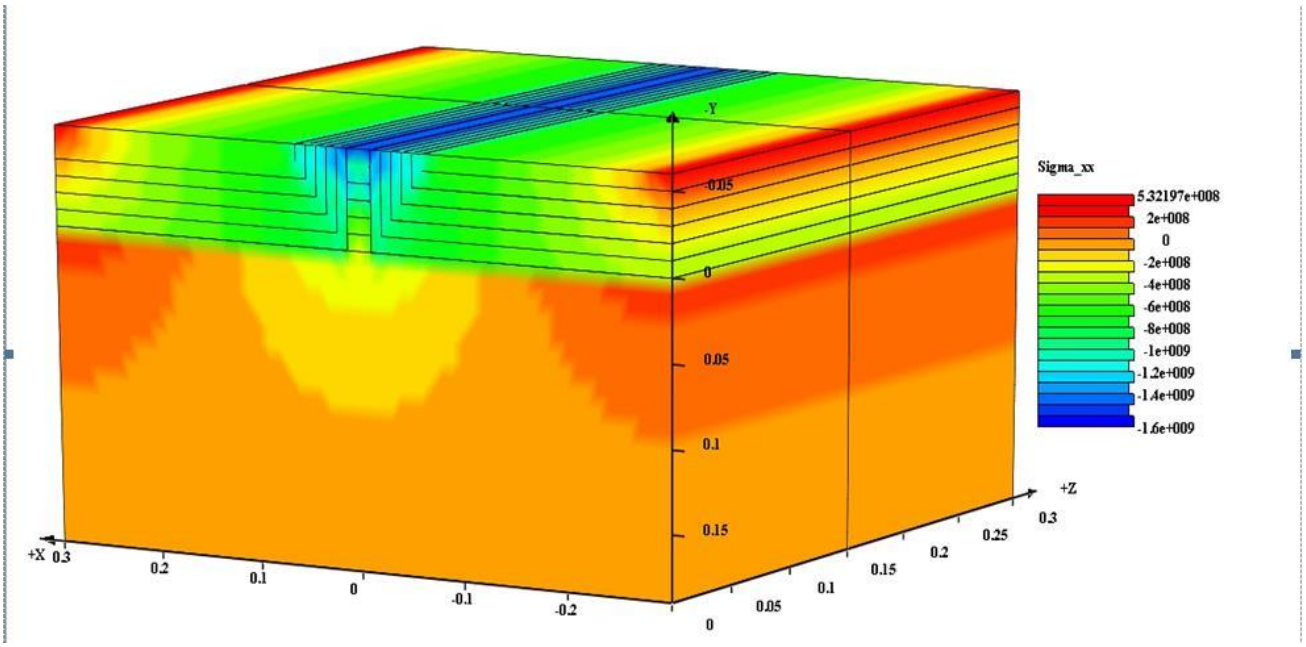

Figure 3: Stress along channel without temperature effects on elastic constants.

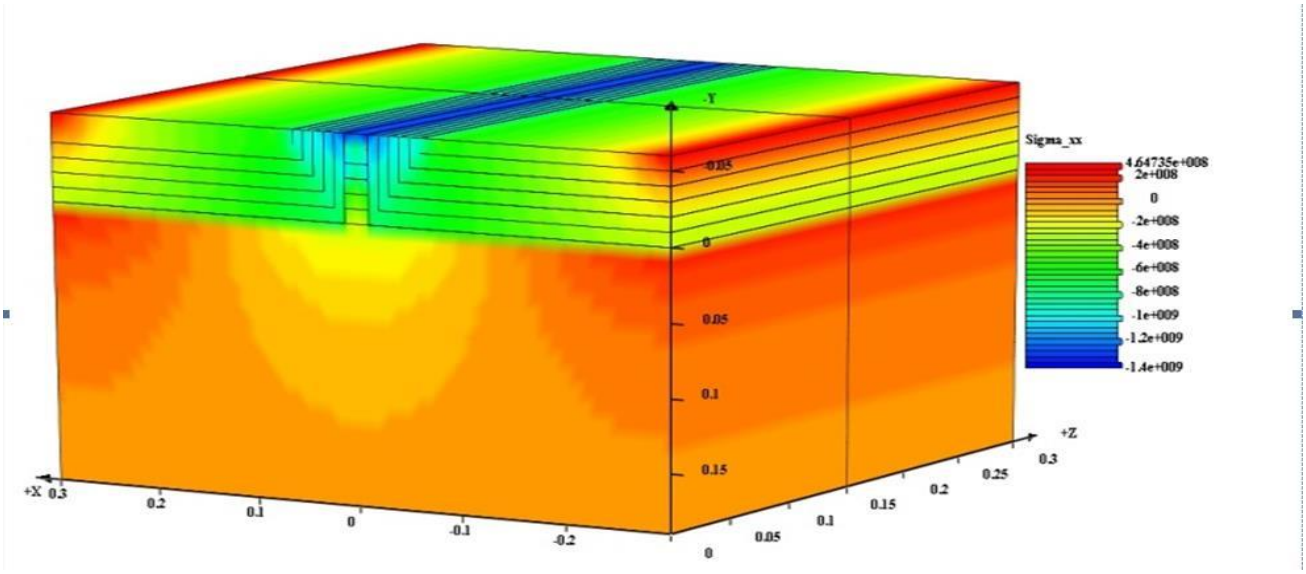

Figure 4: Stress along channel with temperature effects on elastic constants when T=500°C.

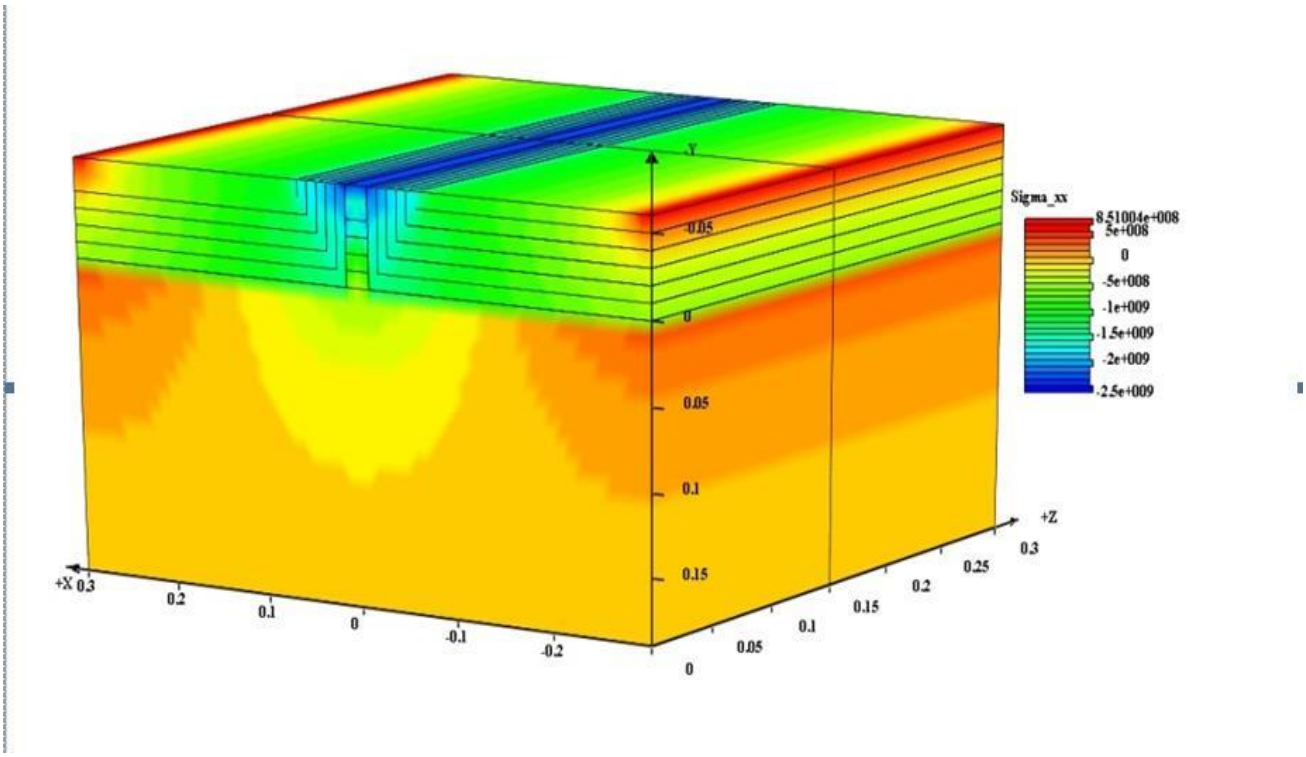

Figure 5: Stress along channel with temperature effects on elastic constants when T=882°C.

Conclusion

The values of stress are overestimated when the effects of the fabrication temperatures are not included in the elastic constants. We can then conclude that to get accurate and correct values of the stress in the channel of a nano pMOS or nMOS transistor, we should take into account the effects of the fabrication temperatures on the elastic constants. In this way, we will get accurate predictions on the electrical performance of nanotransistors used in every area of opto-electronic industry. In the future work, we will investigate the effects of doping on the elastic constants as well.

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Biography

Abderrazzak El Boukili received both PhD degree in Applied Mathematics in 1995, and MSc degree in Numerical Analysis and Scientific Computing in 1991 at Pierre et Marie Curie University in Paris-France. He received BSc degree in Applied Mathematics and Computer Science at Picardie University in Amiens-France. In 1996 he had an industrial Post-Doctoral position at Thomson-LCR company in Orsay-France. He worked on Drift-Diffusion models to simulate transistors for radar applications. In 1997, he had Post-Doctoral position at University of Pavia-Italy. He worked as research engineer on simulation and modeling of quantum effects in hetero junction bipolar transistors for mobile phones. In 2000, he was Assistant Professor and Research Engineer at the University of Ottawa-Canada. Through 2001-2002 he was working at Silvaco Software Inc. in Santa Clara, California-USA as senior Software Developer, on modeling and simulations of vertical cavity surface emitting lasers. Between 2002-2008, he was working at Crosslight Software Inc. in Vancouver-Canada as senior Software Developer on 3D Process Simulation and Modeling. Since Fall 2008, he is working as Assistant Professor of Applied Mathematics at Al Akhawayn University in Ifrane-Morocco. His main research interests are in industrial TCAD software development for simulations and modeling of opto-electronic devices and processes.