Proceedings of the 8th North American International Conference on Industrial Engineering and Operations Management, Houston, Texas, USA, June 13-16, 2023

Analyzing the Operational Parameters of a Single Walled Carbon Nanotube Field Effect Transistor (SWCNT-FET)

S M Shakil, Muhammad S. Ullah
Department of Electrical and Computer Engineering
Florida Polytechnic University
Lakeland, Florida, USA
sshakil2152@floridapoly.edu, mullah@floridapoly.edu

Abstract

Gordon Moore, the co-founder of Intel, predicted that the number of transistors would quadruple every two years. As a result, device scaling had to happen. Scientists and researchers quickly learned that silicon MOSFETs had a scaling issue with technology. Carbon nanotube field effect transistors (CNTFET) are now replacing silicon metal oxide semiconductor field effect transistors (MOSFET) as an alternative. However, whereas we have access to precise circuit-level equations for MOSFETs, all we have for carbon nanotubes are model equations. In this research, we seek to model the behavior of the SWCNT-FET under varying conditions of diameter and gate insulator thickness. This would allow for more accurate performance predictions from the device, paving the way for more complicated CNTFET based circuit designs. Variations in mobile charges, drain currents, and gate insulator thickness are among the variables investigated. Simulation results demonstrate that the size of CNT diameter has direct influence on drain current which could be potential replacement of silicon technology for digital applications.

Keywords
MOSFET, Carbon nanotube, SWCNT-FET, Technology Scaling.

1. Introduction

The concept of mounting many electronic devices on a single substrate emerged in the late 1950s. Over the last six decades, we have gone from making basic circuits with only a few components to making microprocessors with 10 million devices and memory that can hold more than a billion transistors (Shakil and Ullah., 2022). Computer and communication technology have revolutionized every facet of contemporary life because of Moore's law, which states that the number of transistors in general-purpose microprocessors will roughly double every two years (Amin et al., 2019; Ullah et al., 2017). This rule was first proposed in the 1960s. Moore's law predicts that as transistor sizes continue to decrease exponentially, the cost, speed, and energy consumption of modern computers and other information processing equipment will also continue to decrease (Shabir and Ullah., 2022). The advancements made thus far are remarkable; today's smartphones' central processing units (CPUs) are more than 100,000 times more powerful than the Apollo computer that landed a man on the moon 50 years ago while using less than ten times as much electricity. By allowing computers to feasibly handle huge amounts of data with tolerable throughput and cost, the most recent advances under Moore's law paved the basis for today's achievements in machine learning and blockchains (Debnath et al., 2023).

For instance, higher-precision and cognitive learning and inference tasks, whether on the cloud or at the edge, necessitate faster and more energy-efficient computers to train and execute increasingly complex deep-neural network models (composed of hundreds of thousands of nodes and thousands of millions of parameters) (Shabir et al., 2022). Since the difficulty of mining blockchains rises exponentially with the number of nodes in the network, commercial blockchain applications need hardware with a much greater hash rate. To enhance mobility and the user experience, virtual- and augmented-reality applications need greater computer power with much reduced battery consumption on mobile devices (Shakil and Rashid., 2023). Some of these issues can be addressed by software and architectural enhancements, but it would be preferable if transistor technologies could provide a reduced footprint and greater performance on the device level (an approach termed more Moore) (Shakil and Ullah., 2023).

The semiconductor industry's development has slowed over the last decade, indicating that Moore's law, which is based on the scaling of silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), is reaching its physical

limitations (Shakil and Ullah., 2023). To begin, while the number of transistors in modern microprocessors has maintained its exponential development trajectory, both the clock frequency and the chip's single-thread performance have plateaued since the early 2000s (Fig. 1(a)). Second, progress in reducing the size of individual transistors has slowed down, with the shortest allowable space between the gates of neighboring transistors on chip (the contacted-gate pitch) decreasing by only approximately 10% from the 10 to the 5 nm technology node (Fig. 1(b)). However, emerging applications are placing a greater emphasis on the need for ongoing improvements in processing capacity.

In 1930, J.E. Lilenfield invented the first MOSFET (metal-oxide-silicon field effect transistor). Due to its excellent electrical characteristics, the carbon nanotube field effect transistor is one of the most promising alternatives to replace existing MOSFET technology (Iijima et al., 1991). High on-currents have been shown in carbon nanotube field-effect transistors (CNTFETs), a form of the molecular transistor. Because of the growing difficulty of scaling, advances in materials are becoming more crucial to maintaining Moore's law. At the 45 nm technology node, we have seen the replacement of SiO2 gate dielectrics and polysilicon gates with HfSiON-La2O3 high-k gate dielectrics and metal gates, as well as the replacement of aluminum with copper interconnects at the 180 nm technology node (Sumio et al., 1992). The silicon channel is next in line for the approach. Due to their combination of inherent nanoscale size and remarkable electrical capabilities, single-walled carbon nanotubes (SWNTs) stand out as a promising contender among many other possible materials, such as III-V semiconductors and different 2D nanomaterials (Amin et al., 2022; Sanaullah et al., 2014). This review provides an overview of the rationale for using carbon nanotubes instead of silicon in the next generation of extremely scaled logic transistors, a summary of the recent progress made by researchers in academia and industry in transforming nanotube transistors into operational technology, and an examination of the most critical obstacles that must be overcome before this technology can be widely adopted (Figure 1).

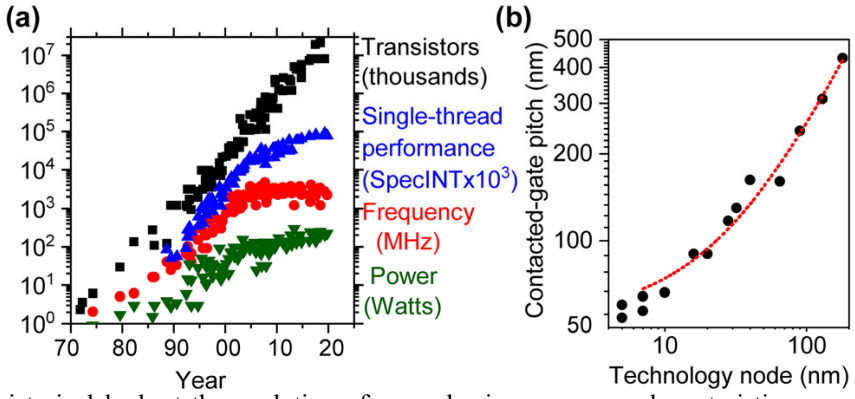

Figure 1. (a) A historical look at the evolution of several microprocessor characteristics over the last 48 years, including the number of transistors (black), single-thread capability (blue), clock speeds (red), and overall power consumption (green) (from Karl Rupp's 48 Years of Microprocessor Trend Data). (b) The technology node scaling behavior of the contacted-gate swing of logic transistors from 180 to 5 nm (source: Wikichip).

2. Properties of Carbon Nanotubes

Carbon nanotubes, also known as "nanotubes," are cylinder-shaped structures made by rolling graphene sheets in an axial orientation (Koyama et al., 1974). Depending on the number of times the graphene sheet is rolled, CNTs are either single walled (SWNT) or multi-walled (MWNT). Nanotubes may have either a zigzag, armchair, or chiral structure, depending on the direction of the rolling vector (chiral vector) (Shabir et al., 2023). The production method for carbon nanotubes determines their final physical, chemical, and optical characteristics. Rolling graphene sheets in an axial orientation creates carbon nanotubes, also known as "nanotubes," which are cylinder-shaped structures. Depending on the number of times the graphene sheet is rolled, CNTs are either single walled (SWNT) or multi-walled (MWNT) (Amin et al., 2020; Sanaullah et al., 2014). Nanotubes may have either a zigzag, armchair, or chiral structure, depending on the direction of the rolling vector (chiral vector). The production method for carbon nanotubes determines their final physical, chemical, and optical characteristics.

In 1993, high-resolution transmission electron microscopy (TEM) provided the first direct evidence that an SWNT's structure resembled a rolled-up sheet of single-layer graphene with a diameter of around 1 nm (Iijima and Ichihashi., 1993). Rapid theoretical and experimental confirmation of SWNTs' extraordinary electrical characteristics followed.

Initial excitement to deploy nanotube transistors as the next switch beyond silicon MOSFETs in the 2000s stemmed from carbon nanotubes' carrier mobility being more than 30 times greater than that of silicon, allowing ballistic carrier movement at ambient temperature across several microns (Debnath et al., 2023). Despite their outstanding nature, these features do not address the critical issues that must be resolved in a scaled logic transistor.

2.1 Electrical Properties

The band structure of graphene simplifies the study of the electrical characteristics of carbon nanotubes. We found that the only allowed k-points in the Brillouin zone are along parallel lines by analyzing the band structure using the

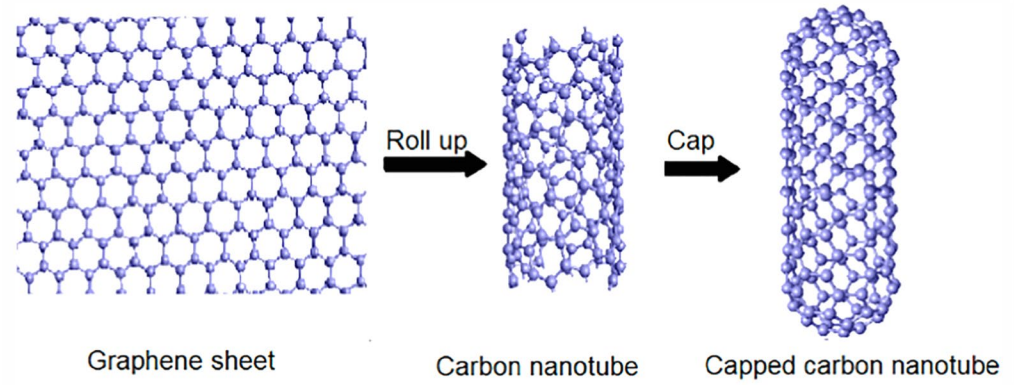

Figure 2. Technique for fabricating carbon nanotubes from single-layer graphene (Shabir and Ullah., 2022).

zone folding approximation. The band structures of graphene, p-type, and n-type nanotubes are shown in Figure 2, together with their electronic energies along the permissible lines. The length and orientation of these lines are designated by the (n, m) pair of integers (dang et al., 2006). Although this approximation has its limitations, it does provide us with a wealth of useful information about the electrical properties of carbon nanotubes, such as the fact that a slight adjustment to the parameters can transform CNTs from a metallic to a semi-conductive state (Shabir and Ullah., 2022).

Carbon, the building block of graphite, has a pair of 1 electron, one 2p electron, and three SP2 electrons in each atomic structure. As a result of the three bonds formed by the sp2 electrons in the band at the sheet plane of graphene, the p-orbital is unsaturated. The delocalized p-network across the nanotube is responsible for its electrical characteristics, and this p-orbital, which is perpendicular to the graphene and hence the nanotube surface, is responsible for its generation. Band degeneracy between the highest p valence band and the lowest p conduction band is required for armchair CNTs to exhibit metallic behavior. At the Fermi level, when these bands overlap, a new kind of CNT called metallic nanotubes is formed (Amin et al., 2020; Santos et al., 2019). Regarding the effect of gate voltage, ballistic conduction in metallic CNTs is the least sensitive. In Fig. 4, we can see how the small band gap of semiconducting nanotubes might be useful in transistor and Fig. 3 shows CNTs applications.

2.2 Chemical Properties

The pyramidal perspective According to the band structure, nanotubes have zero HP since their bonds are sp2. According to studies by (Devi et al., 2013) and (Chen et al., 2007), a carbon atom's angle of pyramidalization is close to tetrahedral, coming in at 11.60 instead of zero. The nanotube's sidewalls are only pyramidal zed at an angle of 60 degrees; therefore, its tubular form causes strain. A p-orbital mismatch is responsible for the strain in a nanotube (Shabir and Ullah., 2022). The end cap is very reactive because of its high pyramidalization angle, whereas the side walls are less reactive because of their low angle (Lee et al., 2015).

Stone wall-like structural flaws in nanotubes may be added during synthesis to confer SP2 character to the hexagonal network of tubular nanostructures (Figure 3 and 4). Imperfect nanotubes are more reactive, resulting in enhanced gas adsorption and a quicker rate of functionalization (Shabir and Ullah., 2022).

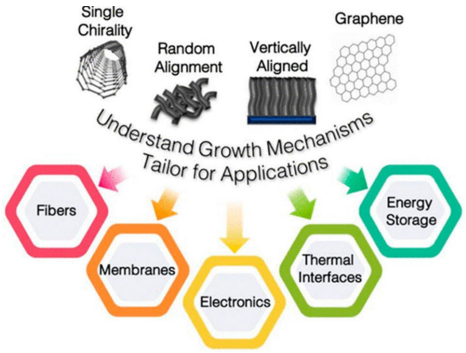

Figure 3. Application of CNTs.

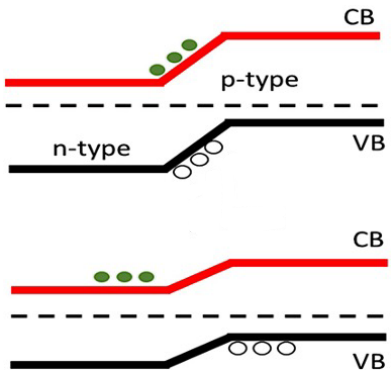

Figure 4. Energy band level variation.

3. Device Structure

The structure of a typical cylindrical CNTFET device is shown in Figure 5. (a) Carbon nanotubes, with a diameter of dcnt, form the innermost tube. The CNTFET has a metal gate that is the outermost tube. The device's behavior depends on whether it is ballistic or diffusive due to dispersion inside the nanotube. We assume that the resistance of the metal to the nanotube contact is zero. Because of the inclusion of ballistic circumstances, the channel length is irrelevant.

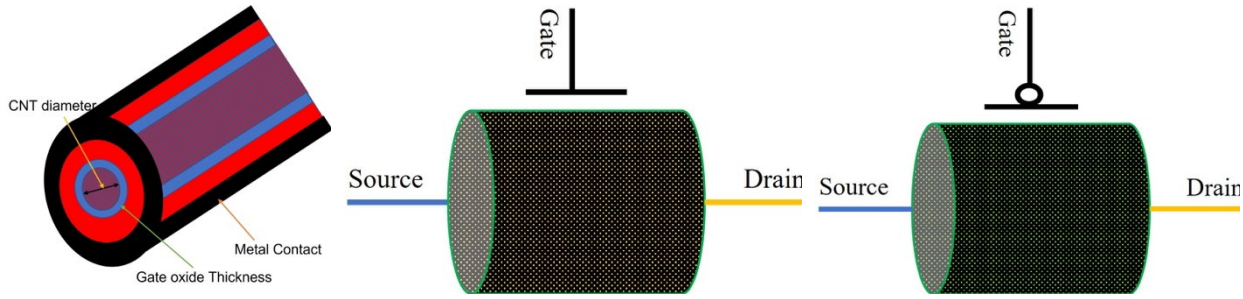

Figure 5. (a) Cylindrical structure of CNTFET. (b) n-type compact model. (c) p-type compact model of CNTFET

3.1 Benefits of CNTFETs

- I(on)/I(off) ratio is quite high.
- Higher threshold voltage.
- It has a very high transconductance. Each FET's performance is based on this characteristic. Gain of the output current increases as transconductance rises (Franklin., 2013).
- It is possible to use CNTs to construct connections with low resistance and great strength.
- Carbon nanotube field-effect transistors (CNTFET) are low-power and highly scalable (Shabir A., 2023).

3.2 Compact Models

Figures 5 (b) and (c) are miniature representations of n-type and p-type CNTFETs, respectively. They help with the visual representation of circuits on paper. Using the CAD tool, we ran simulations to predict how a single-walled carbon nanotube FET might function. We settled on the nanotube's diameter (dcnt) and the thickness of the gate insulator as the independent variables of interest. Several variables, including drain current, mobile charges, quantum capacitances, etc., were investigated. Let us start by experimenting with different nanotube diameters to see what happens.

4. Analysis of Simulations and Discussions

In this section we are going to analyze the simulation results and discuss the variables parameters which effect the characteristics of CNTFET.

4.1 Carbon Nanotube Diameter (Dcnt) as Setting Parameter

The primary formula for determining the diameter of CNTFET (Lee et al., 2015) is given below.

$$dcnt = \frac{\sqrt{3}*a}{\pi}\sqrt{n^2 + m^2 + nm} \quad (1)$$

For a given diameter dcnt of a CNT, we need to know the distance between carbon atoms and the basis vectors a1 and a2 of the graphene sheet, and the chairal index n and m. Where dcnt be the diameter of the CNT, a is the carbon-carbon atom distance and n, m is chairal index using basis vector a1 and a2 of the graphene sheet.

The formula for determining the threshold voltage (Lee et al., 2015) is as follows:

$$Vth = \frac{E_g}{2*e} = \frac{\sqrt{3}}{3} * \frac{\propto * V_\pi}{e*dcnt} \quad (2)$$

Where E_g is the energy band gap, e be the unit electron charge and $V_\prod$ is the carbon $\prod$-$\prod$ bond. There is a correlation between nanotube diameter and threshold voltage. The nanotube's threshold voltage is proportional to its tube size. The investigation of CNTFETs reveals, among other things, that the threshold voltage varies with device diameter. The default values for the simulation's primary variables are listed in Table 1.

Table 1: Node Parameters for Simulation

Gate oxide insulator thickness	2 nm
Gate insulator dielectric constant	2.8
Threshold voltage	0.30V
Gate control parameter	0.80
Drain control parameter	0.030
Series resistance (ohm-um)	0
Ambient temperature	300K

4.1.1. Drain Current VS Gate Voltage

Figure 6 illustrates how changing the FET's diameter affects the drain current and gate voltage. According to the threshold voltage equation (2), there is a negative correlation between the CNTFET's width, and the voltage required to turn it on. The threshold voltage rises as the diameter becomes smaller. Consequently, as the diameter of the FET decreases, the gate voltage required to make it conduct increases. Due to the FET's delayed conduction for smaller diameters, drain current also decreases as carbon nanotube diameter is reduced.

4.1.2. Mobile Charges VS Gate Voltage

For drain current to flow through the channel, or carbon nanotube, there must be enough mobile charges. As demonstrated in Figure 7, the mobile charges grow exponentially with increasing gate voltage. Now it is clear from the curve that as the nanotube's diameter decreases, there will be less room for charges to flow, reducing their total number. From these equations, we can derive an alternative explanation for why the threshold voltage rises monotonically with decreasing nanotube diameter. Therefore, the nanotube would need a high gate voltage to begin conducting.

4.1.3. Mobile Charges VS Drain Voltage

Figure 8 depicts the results of our simulations, which show the relationship between mobile charges and drain voltage for four different diameters and a gate voltage of 1V. When the diameter is only 0.05 nm, the mobile charges remain constant regardless of the drain voltage. By increasing the diameter to 1 nm, we can see that the mobile charge saturates at roughly 0.6 volts on the drain side for a voltage applied to the gate of 1 volt. Therefore, it is reasonable to infer that a circumference of at least 0.5 nm and a respectable gate voltage are necessary to obtain an appreciable number of mobile charges.

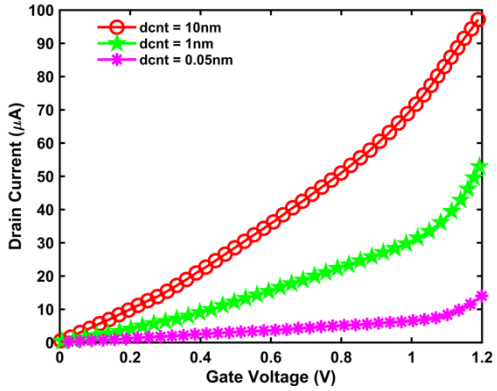

Figure 6. Drain current vs Gate voltage

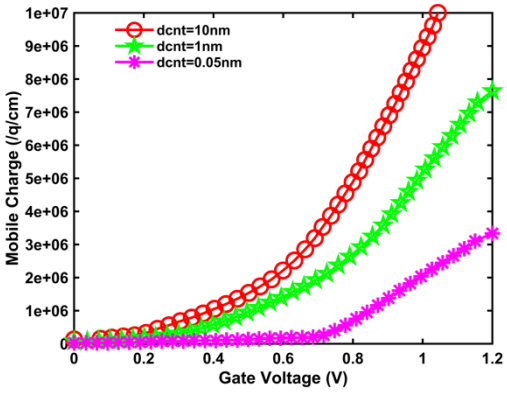

Figure 7. Mobile charge vs Gate voltage

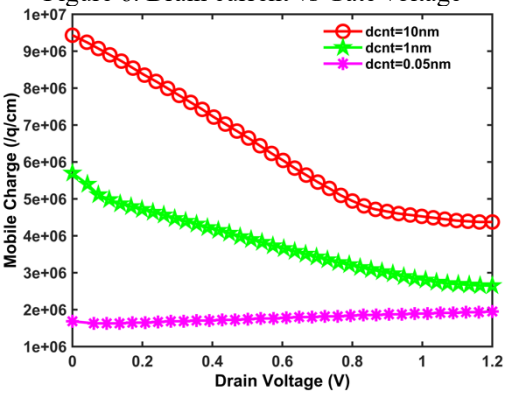

Figure 8. Mobile charge vs Drain voltage

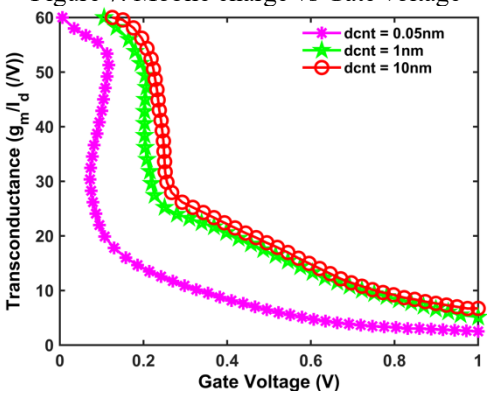

Figure 9. Transconductance vs Gate voltage

4.1.4 Transconductance VS Gate Voltage

Figure 9 shows a graph of the gm/Id ratio, which tells us that a small diameter is required to maintain a high transconductance for a long enough duration to be useful. This is because a bigger gain at the output current Id would be achieved with a larger transconductance.

4.2 Gate Insulator Thickness as Setting Parameter

In this section we are going to discuss the impact of gate insulator thickness of a CNTFET in the below. The default values for the simulations are shown in Table 2.

Table 2: Node Parameters for Simulation

Diameter of nanotube (dcnt)	1nm
Gate insulator dielectric constant	2.8
Threshold voltage	0.30V
Gate control parameter	0.80
Drain control parameter	0.030
Series resistance (ohm-um)	0
Ambient temperature	300K

4.2.1 Drain Current VS Gate Voltage

Figure 10 depicts the drain current's dependence on the gate voltage for CNTFETs with varying gate insulator thickness. The current capability continues growing as we continue to reduce the gate oxide thickness. This demonstrates that when we reduce the thickness of the gate insulator, the FET's conductivity improves.

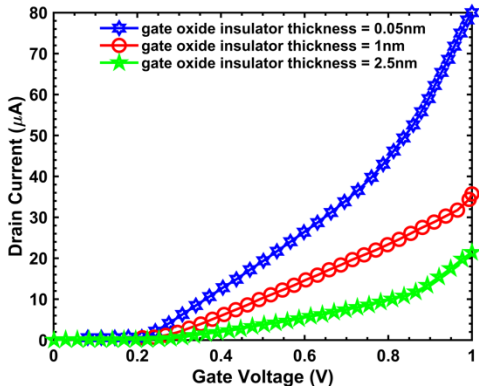

Figure 10. Drain current vs Gate voltage

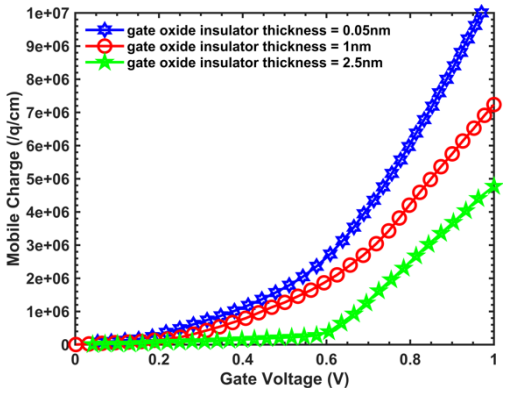

Figure 11. Mobile charge vs Gate voltage

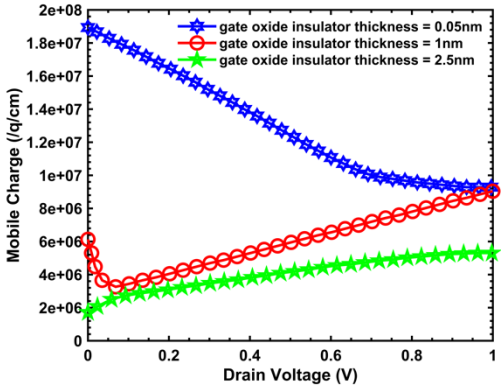

Figure 12. Mobile charge vs Drain voltage

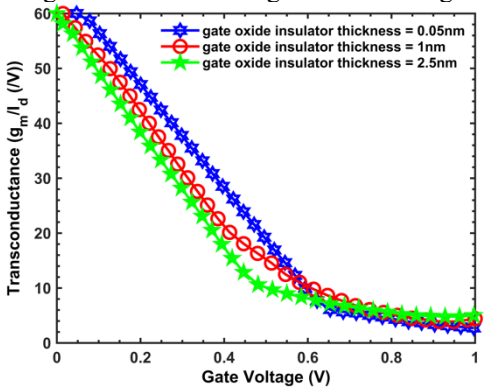

Figure 13. Transconductance vs Gate voltage

4.2.2 Mobile Charges VS Gate Voltage

Bringing the gate insulator down in thickness increases the mobile charges, as seen in Figure 11. Because of this, both the drain current and the maximum allowable current have gone up.

4.2.3 Mobile Charges VS Drain Voltage

Our calculations for mobile charges against drain voltage at a gate voltage of 1V and four different insulator thicknesses for the gate are shown in Figure 12. Changes in mobile charges are highly noticeable for gate insulator thicknesses as little as 0.05nm. The mobile charges begin to level out regarding the drain voltages as the gate insulator thickness grows. As a result, the relationship between the nanotube's diameter and the thickness of its gate insulator is counterclockwise.

4.2.4 Transconductance VS Gate Voltage

Figure 13 depicts the gm/Id ratio as a graph. The gate insulator thickness of a CNTFET must be low for it to produce a significant transconductance. If the transconductance is high, the gain at the Id output current will also be high. The findings demonstrate an increasing gm/Id ratio due to an increasing gate oxide capacitance when the gate insulator thickness is decreased.

5. Conclusion

The carbon nanotube FET's behavior has therefore been characterized by a range of input values. The graph of the mobile charge vs the gate voltage reveals that the current carrying capacity of a nanotube decreases as its diameter decreases, whereas the current carrying capacity of a nanotube with a thinner gate insulator increases. Both the nanotube's diameter and the thickness of the gate insulator have an impact on the relationship between the drain voltage and the drain current. In the future, it may be possible to determine the device's gain by analyzing other metrics, such as quantum capacitances and transconductances.

References

Iijima S. *et al.*, "Helical microtubules of graphitic car- bon," *nature*, vol. 354, no. 6348, pp. 56–58, 1991.

Amin. A. B. and Ullah M. S., "Mathematical Framework of Tetramorphic MWCNT Configuration for VLSI Interconnect," in IEEE Transactions on Nanotechnology, vol. 19, pp. 749-759, 2020, doi: 10.1109/TNANO.2020.3026609.

Sumio I. *et al.*, "Smallest carbon nanotube," *nature*, vol. 358, no. 6381, 1992.

Koyama T., Endo M., and Hishiyama Y., "Structure and properties of graphitized carbon fiber," *Japanese Journal of Applied Physics*, vol. 13, no. 12, pp. 1933–1939, 1974.

Shakil S. M. and Rashid M. H., "The Potential Impacts of Wireless Power Transfer on the Global Economy, Society, and Environment," 2023 14th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Babol, Iran, Islamic Republic of, 2023, pp. 1-5, doi: 10.1109/PEDSTC57673.2023.10087180.

Iijima S. and Ichihashi T., "Single-shell carbon nanotubes of 1-nm diameter," *Nature*, *363*, 603–605, 1993.

Dang T., Anghel L., and Leveugle R., "Cntfet basics and simulation," in *Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006. International Conference on*. IEEE, pp. 28–33, 2006.

Shakil S M., and Ullah M. S., "Reliability Issues in Current MOSFET and Beyond Silicon Technology," *Proceedings of the 8th North American International Conference on Industrial Engineering and Operations Management (IEOM 2023)*, Houston, Texas, USA, 13 -15 June 2023, Accepted.

Shabir A., and Ullah M., "Heat transfer characteristics of CNT with chirality engineering for solar cell application," *In 2022 IEEE International Semiconductor Conference (CAS 2022),* Barsov, Romania, 12-14. October 2022, pp. 159 -162.

Shakil S. M and Ullah M. S., "Analysis of HCD Effects for NMOS Transistor with Technology Scaling," In *IEEE SoutheastCon 2023*, Orlando, USA, 14-16 April 2023, pp. 445-449, doi: 10.1109/SoutheastCon51012.2023.10115193.

Santos J. A., T. F. Kelly, and M. S. Ullah, "Exploring Carbon Nanotubes for VLSI Interconnects," 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS), Dallas, TX, USA, 2019, pp. 1122-1126, doi: 10.1109/MWSCAS.2019.8885390.

Amin. A. B. and Ullah M. S., "Performance Analysis of Squarely Packed Polymorphic SWCNT Interconnect," 2019 IEEE 10th Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON), New York, NY, USA, 2019, pp. 1199-1203, doi: 10.1109/UEMCON47517.2019.8992975.

Sanaullah M. and M. H. Chowdhury, "A new real pole delay model for RLC interconnect using second order approximation," 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, USA, 2014, pp. 238-241, doi: 10.1109/MWSCAS.2014.6908396.

Shabir A., and Ullah M., (2022) "Chirality Engineering on CNTs - A New Approach to Boost the Solar Cell Efficiency," *Proceedings of the 7th North American International Conference on Industrial Engineering and Operations Management (IEOM 2022)*, Orlando, USA, 11 -14 June 2022, pp. 1705-1706.

Chen C., Hou Z., Liu X., E. Siu-Wai Kong, J. Miao, and Y. Zhang, "Fabrication and characterization of the performance of multi-channel carbon-nanotube field-effect transistors," *Physics Letters A*, vol. 366, no. 4, pp. 474– 479, 2007.

Shabir A., "Design of MR Damper for Automobile suspension with finite Element Method," *Proceedings of the 8th North American International Conference on Industrial Engineering and Operations Management (IEOM 2023)*, Houston, Texas, USA, 13 -15 June 2023, Accepted.

Franklin, A. D. The road to carbon nanotube transistors. *Nature*, *498*, 443–444, 2013.

Amin, Abu Bony, Syed Muhammad Shakil, and Muhammad Sana Ullah. 2022. "A Theoretical Modeling of Adaptive Mixed CNT Bundles for High-Speed VLSI Interconnect Design" *Crystals* 12, no. 2: 186. https://doi.org/10.3390/cryst12020186

Shakil S. M and Ullah M. S., "Effects of NBTI On PMOS Device with Technology Scaling," *2022 IEEE 13th Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON)*, New York, NY, NY, USA, 2022, pp. 0402-0406, doi: 10.1109/UEMCON54665.2022.9965669

Amin. A. B. and Ullah M. S., "Performance Analysis of Squarely Packed Dimorphic MWCNT Bundle for High-Speed VLSI Interconnect," 2020 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), London, ON, Canada, 2020, pp. 1-6, doi: 10.1109/CCECE47787.2020.9255744.

Sanaullah M. and M. H. Chowdhury, "Analysis of RLC interconnect delay model using second order approximation," 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, VIC, Australia, 2014, pp. 2756-2759, doi: 10.1109/ISCAS.2014.6865744.

Shabir A. and Ullah M., "Investigation of the emerging materials based high efficiency cdte solar cell," *Proceedings of the 7th North American International Conference on Industrial Engineering and Operations Management (IEOM 2022)*, Orlando, USA, 11 -14 June 2022, pp. 2698-2706.

Lee, C. S.; Pop, E.; Franklin, A. D.; Haensch, W.; Wong, H. S. P. A compact virtual-source model for carbon nanotube FETs in the sub-10-nm regime—Part I: Intrinsic elements. *IEEE Trans. Electron Devices*, *62*, 3061–3069, 2015.

Shabir A., Zaidi B., Ullah M., "Carrier Generation Ability of CNTs to Harvest Maximum Energy from Solar Spectrum, In *IEEE SoutheastCon 2023*, Orlando, USA, 14-16 April 2023, In Press.

Shabir A., Cao J., Fouad E., Ullah M., "Prospects of Solar Cell Technology from Silicon to Carbon Nanotubes", *IEEE 9th International SETIT conference,* Sfax Tunisia, 2022.

Debnath Atanu., Uddin MN., et al "Underwater Surveillance Autonomous Boat," *Proceedings of the 8th North American International Conference on Industrial Engineering and Operations Management (IEOM 2023)*, Houston, Texas, USA, 13 -15 June 2023, Accepted.

Shabir, A., and Ullah M., "Explore the chirality engineering of carbon nanotubes for solar cell". *Florida Scientist, vol.85, no.*2, pp. 68, 2022.

Ullah M. S. and M. H. Chowdhury, "Analytical Models of High-Speed RLC Interconnect Delay for Complex and Real Poles," in IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 25, no. 6, pp. 1831-1841, June 2017, doi: 10.1109/TVLSI.2017.2654921.

Devi D., Rakesh P., and Rakesh V., "Impact of Scaling Gate Insulator Thickness on the Performance of Carbon Nanotube Field Effect Transistors (CNTFETs)," *Nano and Electronic Physics*, vol. 5, no. 2, 2013.

Acknowledgements

This work is supported by Florida Polytechnic University Professional Development fund.

Biographies

S M Shakil received a B.S. degree in electrical and electronic engineering from the Dhaka University of Engineering and Technology, Gazipur, Dhaka, Bangladesh, in 2013. He is currently working toward an M.S. degree in electrical and computer engineering at Florida Polytechnic University, Lakeland, FL, USA, under the supervision of Dr. Muhammad S. Ullah. His current research interest focuses on MOSFET Reliability, Carbon Nanotubes for high-speed VLSI interconnects, and Field Effect Transistor. SM also worked on Wireless Power Transfer and Renewable Energy. He is a member of the IEOM Society International and a Graduate Student Member of the IEEE.

Dr. Muhammad S. Ullah, Ph.D. is an assistant professor of electrical and computer engineering at Florida Polytechnic University. His research focuses are the modeling of RLC interconnects in high density integrated circuits and energy-efficient electronic devices (TFET) for logic applications based on emerging 2-D nanomaterials (MoS2, Graphene, and CNT). He also worked on a neural network-based classification of deceptive and stress speech using non-linear spectral and cepstral features during his master's study. In his Ph.D. dissertation, he investigated the high-speed very-large-scale integration (VLSI)interconnect and energy-efficient electronic devices for emerging post-MOSFET and beyond silicon technologies. Before joining Florida Poly, Ullah worked as a full-time lecturer from 2008 to 2011 at the Chittagong University of Engineering & Technology (CUET), Bangladesh. From 2011 to 2013, he worked as a teaching assistant at Purdue University Northwest. He began working as a full instructor at the University of Missouri-Kansas City while he pursued his doctoral degree. He has taught undergraduate courses in electrical circuits, digital logic designs, signals and systems, and graduate courses in advanced digital signal processing, introduction to VLSI designs, advanced VLSI designs, and emerging nanotechnology, including hands-on experience in MATLAB, Cadence Virtuoso, and HSPICE. Dr. Ullah has served as a regular reviewer of many journals and conferences, including IEEE Transactions on very large-scale integration systems, IEEE International Symposium on Circuits and Systems, IEEE Midwest Symposium on Circuits and Systems, Microelectronics Journal-Elsevier and Circuits, Systems and Signal Processing-Springer, and ASP Journal of Low Power Electronics.