# Apply the Tiling Technique of Heterogeneous Computing on Meta-heuristics

## Gary Yu-Hsin Chen

Department of Logistics Management National Kaohsiung University of Science and Technology Kaohsiung 82445, Taiwan garychen@nkust.edu.tw

Ping-Shun Chen Department of Industrial and Systems Engineering Chung Yuan Christian University Chung Li 32087, Taiwan <u>pingshun@cycu.edu.tw</u>

#### Abstract

With its multicore technology designed for intensive computation, graphics processing units (GPUs) have advanced tremendously in recent years. The GPU is a multicore coprocessor with dozens or even hundreds of cores designed for intensive computations, unlike a central processing unit (CPU), which has a limited number of cores available. However, CPUs have large caches for accommodating large amounts of data, whereas GPUs have smaller caches but use a massive amount of threads. In order to achieve the best performance from both CPU and GPU, GPU-CPU heterogeneous computing architectures have emerged, resulting in a paradigm shift in parallel computing. Data parallelism, also known as SIMD (single instruction, multiple data), is realized through this paradigm, which allows multiple threads to execute the same task simultaneously on different subsets of the same data. When data parallelism is used to program, it is particularly relevant when there is a lot of data to process, as is often the case in scientific computing. Due to their inherent nature as intensive computing, data parallelism is ideally suited for meta-heuristics. As part of this research, data parallelism is introduced to meta-heuristics, as well as a particular optimization technique called "tiling" in parallel computing. "Tiling" refers to grouping threads into tiles to share access to programmable caches on GPUs in order to improve computation speed, particularly for programs that use the same data repeatedly. We introduce the "tiling" technique to ant colony optimization, a meta-heuristic for solving quadratic assignment problem (QAP). A heterogeneous computing architecture is expected to provide benefits in speed, quality, and efficiency over a CPU alone.

#### Keywords

Tiling, Heterogeneous Computing, Quadratic Assignment Problem, Ant Colony Optimization, Graphic Processing Unit

### **Biography / Biographies**

**Gary Yu-Hsin Chen** is a full professor in the Department of Logistics Management at National Kaohsiung University of Science and Technology, Taiwan, ROC. He obtained a PhD degree from the Department of Industrial, Manufacturing and Systems Engineering, University of Texas at Arlington, USA. His research area focuses on operations research, meta-heuristics, and software testing and quality assurance.

**Ping-Shun Chen** is a full professor in the Department of Industrial and Systems Engineering at Chung Yuan Christian University, Taiwan, ROC. He obtained a PhD degree from the Department of Industrial and Systems Engineering, Texas A&M University, USA. His research area focuses on network programming or applications, supply chain management, healthcare applications, and system simulation.