A Comprehensive Evaluation of Direct and Indirect Network-On-Chip Topologies

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Abstract

Over the last few years, there has been dramatic need for developing multi-processors with higher processing capability with area constraint. The interconnect topology for the processors make a significant contribution to area and network parameters such as average latency, power consumption, packet loss and buffer size. The current research is aimed at contributing to the field of Networks on-Chip (NoCs) design methodology. Many of the solutions proposed are simply borrowing the architectures and topologies from the interconnection networks for parallel architectures field and integrating them on-chip that can be used making load balance in a NoC. Although many aspects directly related to the on-chip context have been addressed, like load balance and power consumption or clock distribution and synchronization (asynchronous designs), it still appears that the proposed solutions are not fully centered around the "on-chip" context. The proposed research aims at developing a design methodology that fully uses the many other advantages of on-chip context. A construction by example is followed in building the methodology. This paper reviews some direct and indirect NoC topologies and their performance.

Keywords
Network-on-Chip, Network Topologies, Network Architecture, Average Latency,

1. Introduction
In the first generation of system-on-chip (SoC), buses were used to connect the components. However, as more cores are integrated onto a single chip due to technology scaling, bus-based approaches cannot properly deal with communication demands of multi-processor SoC (MPSoC) implementations. The major problem of shared medium approaches is related to the fact that as the number of connected components increases, other characteristics such as the parasitic capacitance, propagation delay, power consumption and arbitration times also go up. Thus, there is limitation in applying shared medium approaches with regard to the number of interconnected cores. Due to limitations for shared medium architectures for hundreds or even tens of cores, a scalable alternative is presented by a network-centric approach, in which packets are routed through an interconnect network (Benini et al. 2002) and (Dally and Bertozzi 2001). This network-on-chip (NoC) topology identifies physical layout and connections between nodes and channels in the network, which is highly effective on overall network cost-performance trade-off. This efficiency is related to the point that the topology is able to determine the number of hops (or routers) a message must transfer and also the interconnect lengths between hops. In fact, the topology enhances the network latency significantly. As energy is incurred when data traverse the routers and links, the effect of topology on hop count contributes to energy consumption. Besides, the topology dictates the total number of different paths between nodes, which is a key factor in ability of the network in spreading out traffic in order to support the bandwidth requirements [4]. An NoCcan route packets with many more interconnected components (Benini et al. 2002) and (Gopalakrishna et al. 2009). In NoCs, energy can be spent more efficiently, higher aggregated bandwidth can be supported and greater scalability can be offered.

There are two topology categories: direct topology and indirect topology. In direct topology, each node has direct point-to-point link to a subset of other nodes in the system, called neighbouring nodes. In indirect topology, each node is connected to an external switch, and switches have point-to-point links to other switches. In this paper we investigate some direct and indirect NoC topologies and compare their characteristics, to obtain better topology and new idea about designing and implementing large NoCs.

2. Network Topology

Network topology is an important factor that determines the way the nodes are laid out physically and how they are in connection to each other via the links existing within the network. The significant properties such as the network's bisection bandwidth are characterized by the topology, which significantly contribute to the determination of the overall throughput. In essence, bisection bandwidth refers to the minimum number of the wires which will be cut if network is divided into two halves. The higher value of the bisection bandwidth, the higher throughput will be under the uniform traffic. For the general-purpose CMPs, selection of the best topology is not easy; it is because, at the design time, the resulting traffic patterns and the running applications are unknown. The general purpose network topologies such as rings (Seiler et al. 2008) and (Kahle et al. 2005) and meshes (Howard et al. 2010) and (Bell et al. 2008) have come to exist as popular selections for the on-chip networks. It was because of various reasons such as ease of physical layout, the router complexity, wire length, and so on. Fundamentally, NoC topologies can be described by a graph $G(N,C)$. First, we define some parameters in Table 1 and then we will describe some architectures.

Table 1:Definition for Parameters

Parameters	Definition
N	Number of switches
C	Number of channels between switches
Core	Number of IP cores
i & j	Number of backbone rings & Number of local switches in each subnet
m & n	Number of columns & Number of rows
degree	Number of ports
LF	Localization Factor is the ratio of local traffic to total traffic
λ	Poisson distribution with rate λ
Injection Rate	Rate of traffic that has been injected by traffic pattern.

2.1 Mesh Topology

Figure 1 shows a NoC in a mesh topology. A switch in mesh network is connected to a certain resource, and to its adjacent neighbor switches. The number of switches and the number of resource are the same since only one resource is connected to a switch. It can be seen that all switches except those on the edge of the topology are connected to the four closest switches and the target resource block. The mesh architectural layout enables the system to be divided into processing or resource areas (Ezhumalai et al. 2011). The performance of the mesh layout in terms of average latency with different injection rates is shown in Table 2.

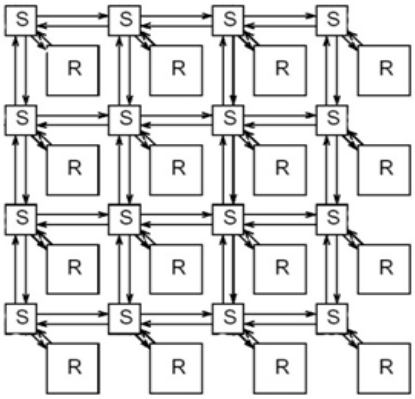

Figure 1: Mesh topology with 16 IP cores

Table 2: Average latency Vs. Injection rate

Injection Rate(Mbps)	Latency (µs)	
	LF = 0.75	*LF = 0.50*
400	2.45	3.25
500	2.50	3.30
600	2.50	3.35
700	2.55	3.4
800	2.60	3.45
900	2.75	3.55

Table 3 shows packet loss and physical area with different buffer sizes. The area characteristics is represented by the number of required logic gates.

Table 3: Packet Loss and area consumption Vs. Buffer Size

Buffer Size	Packet Loss		Number of Gates in ASIC
	LF = 0.75	*LF = 0.50*	
4	2250	2600	270000
6	650	750	340000
8	200	250	400000
10	70	80	450000
12	10	5	500000

2.2 Torus Topology

Torus topology, shown in Figure 2, is similar to the mesh architecture. However, the connection for the switch at the boundary is arranged differently. They are wrapped around from the top switches to the bottom switches and rightmost to leftmost, which leads to the bandwidth of the network being doubled. As a result, such architectural layout gives the chance for a longer transmission distance for a given communication packet (Ezhumalai et al. 2011).

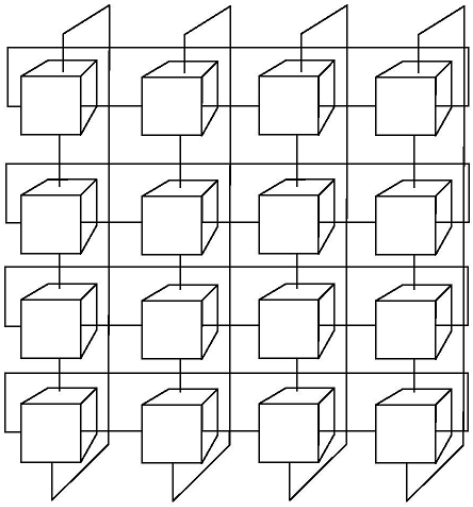

Figure 2: Torus topology with 16 IP cores

The comparison between mesh and torus architectures are described in Eq. (1) - (5).

$$Core_{mesh} = Core_{torus} = m \times n \quad (1)$$

$$Degree_{mesh} = Degree_{torus} = 4 \quad (2)$$

$$N_{mesh} = N_{torus} = m \times n \quad (3)$$

$$C_{mesh} = (m - 1)n + (n - 1)m \quad (4)$$

$$C_{torus} = 2(m \times n) \quad (5)$$

2.3 Norma Topology

Norma is considered as a hierarchical ring-based interconnected topology, in which localized subnets are connected with each other through global routers (switches) in the backbone. As can be seen in Figure 3 and Figure 4, Norma is classified into two types, which are Norma-I and Norma-II (Reza et al. 2008).

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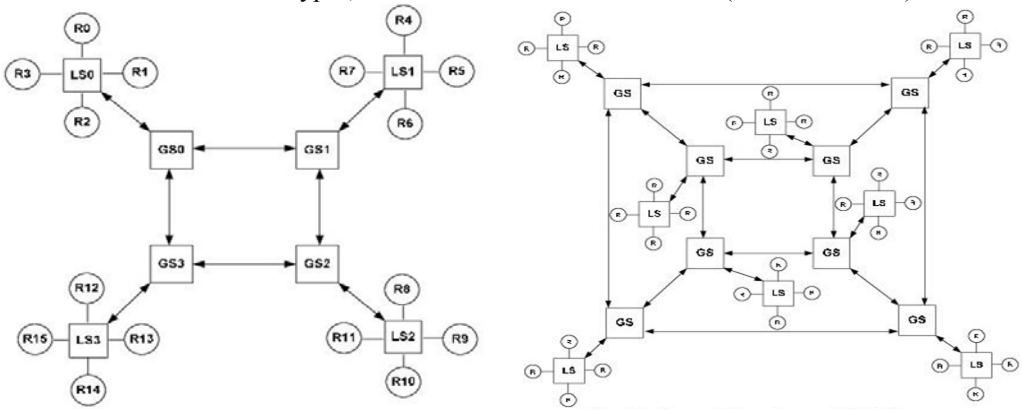

Figure 3: Norma-I topology with 16 IP cores and 32 IP cores

- In Norma-II, multiple routers and resources can be placed in each subnet (Figure 4). Similar to both LS and GS, Norma-II also has just four ports routers (Figure 4).

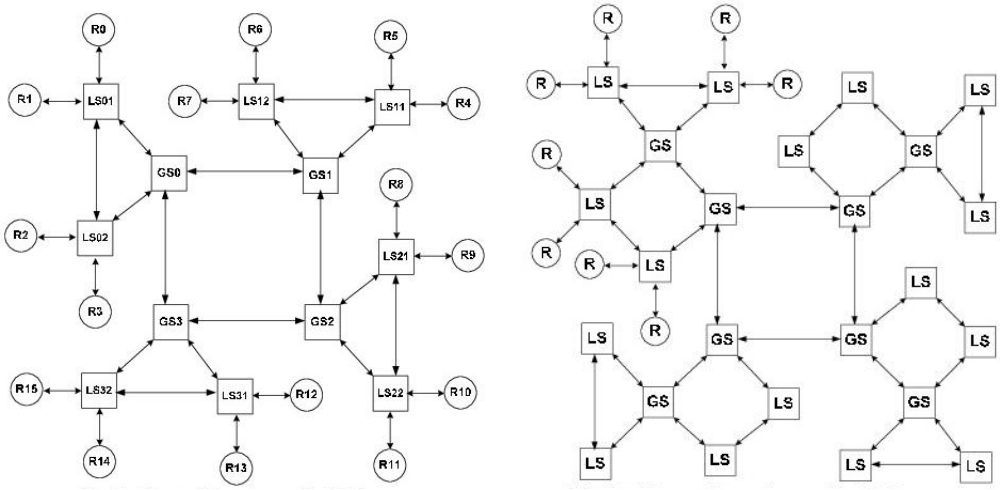

Figure 4: Norma-II topology with 16 IP cores and 32 IP cores

Number of switches (N), number of channel between switches (C) and number of IP cores are calculated in Norma as given by (6) - (11) (Reza et al. 2008).

$$Core_{Norma\text{-}I} = 16 \times i \quad (6)$$

$$N_{Norma\text{-}I} = 4 \times 2 \times i = 8 \times i \quad (7)$$

$$C_{Norma\text{-}I} = 8 + ((8 + 4) \times (i - 1)) = 8 + (12 \times (i - 1)) \quad (8)$$

$$Core_{Norma\text{-}II} = 8 \times j \quad (9)$$

$$N_{Norma\text{-}II} = \begin{cases} 4+4\times(j-2+k_o);\ j=1,3,5,\ldots;\ k_o=1,2,3,\ldots & (10) \\ 4+4\times(j-2+k_e);\ j=2,4,6,\ldots;\ k_e=1,2,3,\ldots & (10) \end{cases}$$

$$C_{Norma\text{-}II} = \begin{cases} 4+4\times(2j-2);\ j=1,3,5,\ldots; & (11) \\ 4+4\times(2j-1);\ j=2,4,6,\ldots; & (11) \end{cases}$$

2.4 Corona Topology

As shown in Figure 7, Corona is a hierarchical architecture and based on an indirect ring topology, in which multiple rings can be connected by four bidirectional links in four main directions (North, West, South, and East). In Corona, every router consists of four ports. Despite this constraint, Corona is able to develop balanced area consumption and operational frequency of routers in all the tiles. In addition, one extra core can be attached to the boundary routers which have two connections with their neighbors in the last outer ring. As a result, there will be modularity through the edges of the topology, in which less power and area is spent which is related to sharing one single router between two IP cores. The hop count reduction causes less average latency of the transactions (Bahmani et al. 2008).

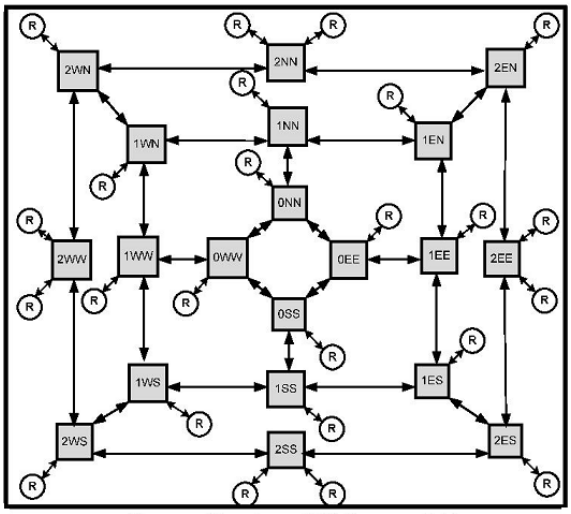

Figure 5: Corona topology

Number of switches (N), number of channel between switches (C) and number of IP cores in Corona are characterized by (12) - (14) (Bahmani et al. 2008).

$$N_{Corona} = 4 + (8\times i);\quad i = 0, 1, 2, 3, \ldots \quad (12)$$

$$C_{Corona} = 4 + (12\times i);\quad i = 0, 1, 2, 3, \ldots \quad (13)$$

$$Core_{Corona} = 8 + (8\times i);\quad i = 0, 1, 2, 3, \ldots \quad (14)$$

Table 4 demonstrates average latency with different injection rates while Table 5 and Table 6 show packet loss and area consumption with different buffer sizes. All three tables compare the performance for Norma and Corona.

Table 4: Average latency Vs Injection Rate

Injection Rate (Mbps)	Latency (µs)					
	LF = 0.75			*LF = 0.50*		
	NormaI	***NormaII***	***Corona***	***NormaI***	***NormaII***	***Corona***
400	1.20	1.40	1.40	2.00	2.45	1.60
500	1.25	1.40	1.40	2.10	2.50	1.65
600	1.30	1.40	1.40	2.20	2.50	1.65

Injection Rate (Mbps)	Latency (µs)					
	LF = 0.75			*LF = 0.50*		
	NormaI	*NormaII*	*Corona*	*NormaI*	*NormaII*	*Corona*
700	1.35	1.45	1.45	2.30	2.55	1.70
800	1.40	1.45	1.50	2.50	2.60	1.80
900	1.50	1.50	1.55	2.80	2.75	1.85

Table 5: Packet Loss Vs. Buffer Size

Buffer Size	Packet Loss					
	LF = 0.75			*LF = 0.50*		
	Norma I	*Norma II*	*Corona*	*Norma I*	*NormaII*	*Corona*
4	1200	650	1300	2800	2200	1900
6	350	290	380	800	650	550
8	120	100	120	300	200	190
10	50	20	40	100	80	80
12	0	0	10	20	0	0

Table 6: Area Consumption Vs. Buffrr Size

Buffer Size	Number of Gates in ASIC		
	Norma-I	*Norma-II*	*Corona*
4	140000	230000	240000
6	170000	285000	290000
8	200000	320000	330000
10	240000	360000	380000
12	260000	425000	415000

2.5 Sphere-Based Topology

Most of the already introduced topologies are based on surface form. However there is also a topology in the sphere shape. In such sphere-based topology, all cores are placed on a sphere shield, which are connected by bidirectional links as shown in Figure 6.

All routers' degrees are 4 except up and down ones that are high radix kind and its degree is 2P. This structure works on connection between axis's (P) and bypass channels loop (Q) with a core at each junction (Nadooshan et al. 2011).

It can be seen that sphere-based topology looks like the torus topology due to existence of bypass channel loops. However, the two radix routers in sphere make it different and cause performance enhancement in contrast to torus topology. Besides, sphere based topology applies simple router (Nadooshan et al. 2011).

Number of cores in a sphere-based topology is given by

$$Core_{Sphere\ based} = 2PQ + 2 \qquad (15)$$

where P is the axis and Q is the number of bypass channel loops candidates, and the 2 represents the two high radix nodes that are placed on top and bottom of the topology (Nadooshan et al. 2011).

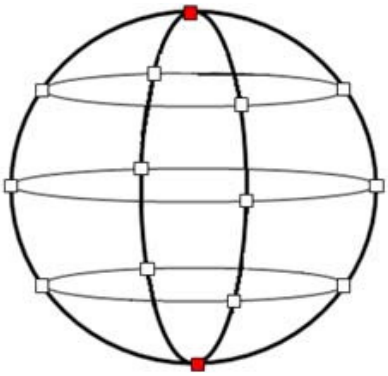

Figure 6: Sphere-based topology with P=2 and Q=3

3. Comparison of Different Architectures

The comparisons performed in this section are based on the topological properties of the different direct and indirect interconnection networks presented in the previous sections. Table 7 shows average latency, degree, average packet loss, power consumption and average cost for topologies which are presented in this paper. Table 8 demonstrates advantages/disadvantages of various topologies compared to mesh and torus topologies. The comparisons are in terms of how much better/worse the topologies with respect to mesh or torus in percentage term.

Table 7: Comparison of Studied Topology

Architecture	**Comparison of studied Architecture**					
	Norma-I	***Norma-II***	***Mesh***	***Torus***	***Corona***	***Sphere***
Avr Latency, LF=0.75 (µs)	1.108	1.433	2.558	-	1.450	-
Avr Latency, LF=0.50 (µs)	2.317	2.558	3.383	-	1.708	-
λ for Avr Latency = 40 (cycles) with 36 IP	-	-	0.0125	0.0225	-	0.020
λ for Avr Latency = 100 (cycles) with 64 IP	-	-	0.0025	0.0050	-	0.065
Degree	3,4,5	4	4	4	4	4
Avr Packet Loss, LF = 0.75	354	212	636	-	370	-
Avr Packet Loss, LF = 0.50	804	626	737	-	544	-
Power consumption (cycles) with 36 IP	-	-	If $\lambda \geq 0.007 \rightarrow pc=4$	If $\lambda \geq 0.012 \rightarrow pc=6.5$	-	If $\lambda \geq 0.01 \rightarrow pc=5.5$
Power consumption (cycles) with 64 IP	-	-	If $\lambda \geq 0.0025 \rightarrow pc=4.5$	If $\lambda \geq 0.006 \rightarrow pc=6.5$	-	If $\lambda \geq 0.008 \rightarrow pc=9$
Avr Cast / Buffer Size	202000	324000	392000	-	331000	-

Table 8: Present average the topology than mesh topology and torus topology

Architecture	**Comparison with Mesh**				**Torus**
	Norma-I	***Norma-II***	***Corona***	***Sphere***	***Sphere***
Avr Latency, LF=0.75	56	44	43	-	-
Avr Latency, LF=0.50	31.5	24	49.9	-	-
Avr Latency = 40 (cycles) with 36 IP	-	-	-	37.5	-11.12
Avr Latency = 100 (cycles) with 64 IP	-	-	-	61.5	23
Avr Packet Loss, LF = 0.75	44	66.5	42	-	-
Avr Packet Loss, LF = 0.50	-9	15	26	-	-
Avr Cast / Buffer Size	48	17	15.5	-	-

4. Large-scale NoC

One of the most important trends in computer architecture in the past decade is the move towards multiple CPU cores on a single chip. Common chip multiprocessor (CMP) sizes today range from 2 to 8 cores, and chips with hundreds or thousands of cores are likely to be commonplace in the future (Borkar 2007) and (Owens et al 2007). Real chips exist already with 48 cores (Intel 2011), 100 cores (Tilera 2011), and even a research prototype with 1000 cores in University of Glasgow (2012). While increased core count has allowed processor chips to scale without experiencing complexity and power dissipation problems inherent in larger individual cores, new challenges also exist. So Network-on-Chip (NoC) has been considered to solve this problem.

Considering the dramatic increase in the number of the nodes inside the networks-on-chip and also the increase in transaction between nodes, the rate of transformation of the data inside the links rises. Thus, some links are likely to be used more excessively than other links which can lead to lack of load balancing inside the NoC. This event makes the packets inside the large NoCs to have long paths to reach the destination. In fact this process takes longer time for a packet to reach the destination resulting in increase in certain parameters such as latency, packet loss and power consumption, and decline in throughput. One of the ways to remove the aforementioned problems is to use routing algorithm. So many routing algorithms were created to solve this problem, but this solution cannot slove completely. However the topologies currently used are good for small size networks only. Thus it is necessary to design and develop new topology which are appropriate for big size NoCs. Besides, the routing algorithm can be optimized to become suitable for the suggested topology. The topology defines how routers are connected with each other and the network endpoints. For a large-scale system, the topology has a major impact on the performance and cost of the network. In order to this, researchers have solved some problems such as routing algorithm, QoS, power consumption, and topology for small NoCs. And Some researchers are working on large NoCs to obtain a solution for problems. For example, in (Nychis et al 2012) authors evaluated large NoC for 16 to 4096 cores. They have shown two important problems in a large-scale NoCs (Figure 7).

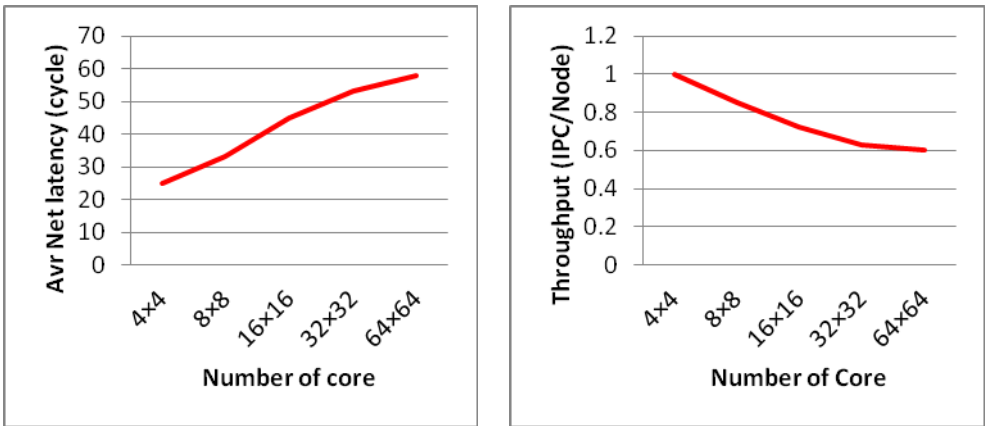

Figure 7: Average Latency and Throughput for different size of mesh topology

5. Conclusion

We have compared different NoC architectures in terms of area, latency, power consumption and packet loss. This comparison indicates that Norma-I has 56% better average latency than mesh and Norma-II has 66.5% better average packet loss than mesh, when they were tested under LF=0.75 and with 16 IP cores. Furthermore, when the number of IP cores increases, the average latency for sphere topology becomes better, when compared with mesh and torus. All of the topologies presented in this paper seemed to be useful for networks. However, there is a question why the researchers did not use them widely, although they gained good results. We notice that the topology optimizations aremostly based on mesh architecture. We are working to design a novel topology for large NoCs, which is ring and mesh based. In future, we will be present new topologies to optimize load balancing and network latency.

Acknowledgements

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Biography

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