Mitigation of WIP-related Problems at an IC Production Line through a Suitable Inspection Sampling Plan

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Abstract

Unpredictable work-in-process (WIP) inventory developed in the inspection area of an integrated circuit (IC) assembly line due to the acceptance criteria dictated by a single sampling plan often requires additional human resources and results in longer production lead time. Sudden need of additional operators to carry out 100% inspection of the rejected lot creates an uneasy and difficult situation for the concerned manager. Securing outgoing quality of the ICs without increasing the production lead time and allocation of additional human resources appears to be a major challenge. Upon a critical study of a real-life assembly line, several sampling plans (double and multiple) which could adequately meet the current average outgoing quality limit (AOQL), a parameter indicating the level of outgoing lot quality, were applied. A multiple sampling plan was suggested to minimize the WIP level with a reduction in consequential effect on the line of operation. The proposed multiple sampling plan is expected to increase the average total inspection (ATI) but the benefits to be accrued through minimization of WIP level and the minimized resources in tackling the situation should outweigh the efforts for additional inspection involving only visual observation without carrying out any expensive destructive tests.

Keywords:
Multiple sampling plan, Work-in-process (WIP), Visual mechanical inspection (VMI), Average outgoing quality (AOQ), IC production

1.0 Introduction

An integrated-circuit (IC) consists of semiconductor wafers on which thousands or millions of gates and other electronic devices are located on a same circuit and compacted to form a single device (T. Noergaard, 2005). Being categorized as either analog or digital an IC can function as an amplifier, oscillator, timer, counter, computer memory or microprocessor, etc. Once wafers are prepared through deposition, removal, patterning, and modification of electrical properties, etc. the next processing step adopted is packaging which starts with the incoming wafer, followed by grinding, die interfacing, die and wire bonding, molding, symbolization, trimming and forming, visual mechanical inspection (VMI), testing and packing prior to shipping to customers. Following the symbol-trim-and-form (STF) operation to the nonconforming (defective) units are sorted out from the lot. The inspection process known as VMI is based on acceptance sampling plan. In a general sense, inspection involves activities such as measuring, examining, testing and gauging characteristics of a product or service and comparing with specified requirements to determine conformity (Stephens, 2001). Sometimes due to involvement of expensive jigs and time, sampling procedures are adopted to avoid inspection of every part (Groover, 2007). Regarding the scope of inspection, W. E. Deming (1986) states that dependency on inspection to correct quality problems is ineffective, costly and should not be used as a long term strategy for quality improvement. Nevertheless, this step cannot be eliminated from production line because inspection acts as a means of control to maintain desired precision and accuracy of product characteristics. Though the inspection work may often be boring and monotonous, yet the need for it as a control mechanism is great and unavoidable.

In IC manufacturing, checking process of product quality is done in the form of (1) manual (2) visual-mechanical (3) test and (4) mechanized / automatic inspection. The VMI mainly focuses on the appearance of the IC chips after finishing operation. Appearance of an IC is as important as its operational function and mechanical perfection. So inspection is intended to detect any lack of merchandising appearance as well as identify the mechanical deficiencies and secure the product quality. Due to the adoption of acceptance sampling plan with 100% rectification in case of lot rejection, there is a scope of unpredictable development of work-in-process (WIP) at the VMI workstation area. In a sampling inspection plan with rectification, a sample is picked randomly from the lot, and the items are checked for conformance. On the basis of data or information yielded by the observation of the sample, a decision is made regarding the disposition of the lot i.e. to accept the lot either without any further action or followed by 100% rectification. Classical acceptance sampling plans have been studied by many researchers. Schilling (1982) has thoroughly elaborated those. Guenther (1984) discussed how to determine the rectifying plans for single sampling by attributes. Suresh and Ramkumar (1996) justified the use of maximum allowable average outgoing quality (AOQ) for developing sampling plan. Single sampling by attributes with relaxed requirements was discussed by some researchers such as Kanagawa and Ohta (1990), Tamaki et al (1991), and Ohta and Ichihashi (1998) whereas Grzegrozewski (2002) considered sampling plan by variables with fuzzy requirements. Benbow, (2003) suggested to determine the type of inspection to be carried out and the acceptable quality level (AQL) to be identified for critical characteristics of defects. But according to Wadsworth (2002), acceptance sampling always incurs certain risks as an entire lot is not inspected, not everything is known. E. B. Jamkhaneh and B. S. Gildeh, (2010) introduces the average outgoing quality (AOQ) and average total inspect (ATI) for double sampling plan when the proportion of nonconforming items is a fuzzy number. As defined by D. C. Montgomery (2005) the AOQ is the quality in the lot that results from application of rectifying inspection. It is the average value of lot quality that would be obtained over a long sequence of lots from a process with fraction defective p.

Generally, IC is processed in large lot size passing through a lengthy operational and testing procedure. Every step in the processing has a significant impact on production lead time. Any problem arising at any processing step can greatly disturb or upset the subsequent operations of the whole line. The location of VMI is a such place of IC production line where there is a scope of unpredictable WIP development and shop floor management often faces challenges in tackling such a situation. As experienced in such an IC manufacturing company, when the defective items in the sample ($n = 600$) taken exceeds the acceptance number, ($c = 5$), 100% inspection is conducted to separate the defective ICs from the lot. When this happens, a high WIP at the VMI is created and it becomes impossible task for the operator alone to complete the inspection work for the rest of the lot within the stipulated cycle time. Under this kind of situation, management requires to mobilize additional human resources to expedite the inspection process.

Arrangement of additional human resources for such a situation turns out to be a recurring problem for the concerned manager. To allocate additional human resources, other workstations are stopped and the operators are released to assist the operator. Thus there prevails a sense of nervousness in the whole production system. Minimizing the frequency of such occurrences without sacrificing the quality of the outgoing ICs as well as the WIP to a tolerable level by engaging a lower level of additional human resource could be a prospective solution. There are a number of research works for reduction of WIP level and its duration. Hamid Ullah (2008) focused on re-assembling a station's goal and presented a new generic Petri net (PN) model based on assembly plan for assembly sequence optimization. However, these concepts are not suitable for the WIP generated due to sampling plan in an unpredictable manner. So this study is undertaken to investigate the possibility of mitigating the extent of the problem. In this regard the current sampling procedure is to be investigated to suggest methods and plans to enhance the operational efficiency by minimizing the inspection WIP at VMI area of IC manufacturing without compromising the outgoing quality level currently set for the purpose of process control. Alternative acceptance sampling plans have been searched and a multiple sampling plan is suggested for implementation to ease the system nervousness prevailing currently in the production system.

2.0 IC Production and Inspection Procedure – Current Situation

The first phase of IC production starts with wafer fabrication which consists of deposition, removal, patterning, and modification of electrical properties. Deposition is a process that grows, coats, or transfers a material onto the wafer. Removal processes are any that remove material from the wafer and consist primarily of etching processes. Patterning, generally referred to as lithography, covers the series of processes that shape or alter the existing shape. Modification consists of doping transistor sources and drains by diffusion furnaces and later by ion implantation. Once the wafers are prepared, the next processing step is packaging to produce the desired semiconductor integrated circuit. In general, the steps in packaging can be grouped into three stages of assembly: Front of Line (FOL), End of Line (EOL) and Test. The FOL also known as 'front-end' refers collectively to early assembly processing steps, i.e., steps prior to molding. The EOL also known as 'back-end' or 'finishing' refers collectively to later assembly processing steps from molding to other succeeding steps. Finally, the Test is a series of checking and testing to determine whether the ICs in the lot comply with all quality specifications and meets customer requirements.

The acceptance sampling procedure that is in place now at the STF of the EOL of IC assembly line is actually a single sampling plan. When production continues, a total of 600 ICs are checked for a typical lot of size of N = 5000 units with an acceptance number, c = 5. Thus about 12% of ICs in the lot are collected from the lot as sample and subjected to screening. Lots that meet the acceptance sampling criteria (when the number of defectives *(d)* in the sample is lower than '*c*' i.e. $d \leq c$) are passed. Lots that fail to meet the acceptance sampling criteria (when value of *d* exceeds *c* i.e. $d > c$) are subjected to 100% inspection. It may be mentioned here that screening of 600 ICs is done at three stages of production. At a time four plastic tube magazines (each contains 50 ICs) are collected and inspected for defective items. So, 200 IC units are inspected in each shot. The procedure of inspection and isolation of defective items is shown in Figure 1.

Figure 1: Use of luxor lamp and magnifier for IC Inspection and procedure of removing defective unit.

Samples are collected at the initial stage of processing the lot, next sample in the middle of processing while third sample of four magazines are screened through at the end phase of the lot processing. Table 1 summarizes the sampling procedure.

Table1: Procedure of sample collection at STF and the sample size

Sequence of Sample taken from a lot	**Magazine and Sample size (n)**
1. First sample – start of the lot	Four tube magazines x 50 IC units = 200 IC units
2. Second sample – middle of lot processing	Four tube magazines x 50 IC units = 200 IC units
3. Third sample – end of lot processing	Four tube magazines x 50 IC units = 200 IC units
Sample size (n) taken for each lot at STF	**Sample size, n = 600 IC units**

As mentioned earlier, since the current acceptance number *(c)* is 5, i.e. if the number of defective items (d) found in the sample exceeds 5, (i.e. d > 5), the lot is rejected and the remaining ICs in the lot are subjected for 100% inspection at VMI. If *d* is less than or equal to 5, the lot is accepted without any further inspection and it is passed to the next process for testing. To reflect the current scenario of process capability, information about the number of lots being accepted on the basis of the current sampling plan and the number of lots passing through 100% inspection have been gathered. Data for one month's production are arranged in sequence of the day of production, lots produced, number of lots accepted on the basis of 100% inspection and the number of lots accepted on the basis of sampling plan. It was observed that 942 lots were produced in the specified month out of which only 31 lots passed through the sampling procedure with 5 or less defective items in the sample of 600 IC units. So only about 3% of the lots are expected to meet the quality level set by the current sampling procedure and 97% of the lots are to pass through 100% inspection. It is obvious that the WIP inventory for VMI is very frequent with a high volume. This huge percentage of lot rejection by the sampling plan indicates that the process capability in terms of maintaining the desired quality level of ICs is quite inadequate. Thus the target set by the sampling plan looks too ambitious and cannot be met by the current production process. To overcome this problem, initiatives should be taken either to improve the whole production process presumably by replacing the old machines with new ones or modify the current sampling procedure to minimize the WIP to mitigate quality control related bottlenecks.

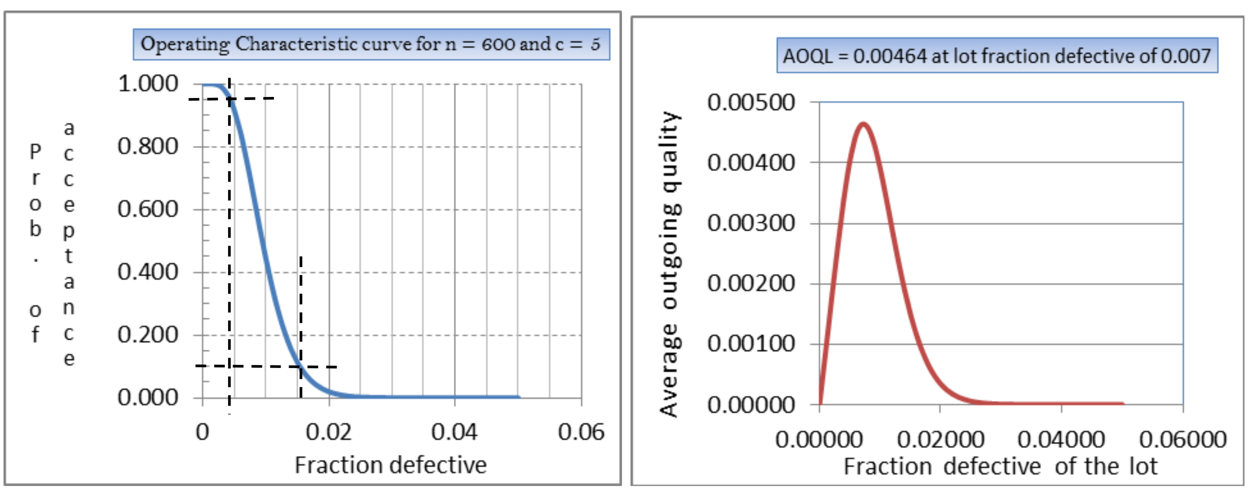
3.0 Proposed Sampling Plan

Replacement of the old machines with the new ones is sometimes unrealistic for a company due to the involvement of prohibitively high costs. So the favourable option remains is modification of the current sampling plan to try to mitigate the turbulent situation or nervousness experienced by the production system due to the unpredictable WIP development. Several measures can be attempted in this regard. Single sampling plan with rectification with bigger sample size having an equivalent Operating Characteristic (OC) curve can be a pragmatic solution. Alternatively, double or multiple sampling plans can also be used. Since with the current plan, the operator (inspector) does not have to remain busy during the whole period of a lot production, the sample size can be increased. Out of 45 minutes available time, the operator hardly remains busy for about 12-15 minutes inspecting 600 IC sample units. To design a suitable sampling plan irrespective of whether this is single, double or multiple, the minimum level of the desirable properties rendered by the current method should be satisfied. Among these characteristics, the acceptable quality level (AQL) and the lot tolerance percent defective (LTPD) representing respectively the producer's risk and consumer's risk are very important. Moreover, average outgoing quality limit (AOQL) is another important parameter to indicate the performance of an inspection plan. The values of AQL, LTPD and AOQL as derived for the current sampling plan may be considered as benchmark and the proposed plans are not be worse in this context.
To derive the OC curve and the relevant sampling parameters, it is necessary to calculate the probability of acceptance as function of fraction defective or process quality, *p.* For this present case, the probability of acceptance, *Pa* is the likelihood that the value of *d* is less than or equal to '*c'* and can be expressed as follows:

$$P_a = P\{d \le c\} = \sum_{d=0}^{c} \frac{n!}{d!(n-d)!} p^d (1-p)^{n-d} \tag{1}$$

The value of *Pa* can be determined for a specified fraction defective *p* using equation 1. In the current sampling plan at VMI, the sample size *n,* is 600 and acceptance number *c,* is 5. So probability of acceptance can be expressed as a function of fraction defective by equation 2.

$$P_a = P\{d \le 5\} = \sum_{d=0}^{5} \frac{600!}{d!(600-d)!} p^d (1-p)^{100-d} \tag{2}$$



(a) (b)

Figure 2: (a) OC Curve and (b) AOQ for Current Acceptance Sampling Plan (*n = 600*, *c = 5*)

The value of AOQ (average outgoing quality) can be determined by using equation 3 as given below:

$$AOQ = \frac{P_a p(N-n)}{N} = P_a p \tag{3}$$

Thus by using equations 2 and 3 the OC and AOQ curves are drawn as presented in Figure 2. In order to determine the AQL and LTPD, two horizontal lines parallel to X-axis are drawn at Pa = 0.95 and Pa = 0.10. The producer's risk, α, and the consumer's risk, β are usually taken as 5% and 10% respectively. Since Pa of a good lot is 95%, the remaining 5% probability of rejecting the good lot is the risk for the producer. On the other hand, the 10% probability of acceptance of a bad lot appears as the risk for the consumer. For the specified values of α, and β, the corresponding fraction defectives have been found as 0.0045 and 0.0153. From Figure 2(b), the maximum value of AOQ i.e. AOQL is determined as 0.00464. These three values actually represent the AQL, the LTPD and the AOQL for the current sampling plan. The important parameters for the current sampling plan are summarized in Table 2.

Table 2: Important benchmark parameters for OC and AOQ curves (n = 600, c = 5)

n	*c*	α	β	AQL	LTPD	AOQL
600	5	0.05	0.10	0.0045	0.0153	0.00464

The above parametric values for the current sampling plan in practice are taken as standard values for designing alternative sampling plans for screening at VMI. Several alternatives from single, double and multiple sampling plans have been simulated for choice. Simulation of OC curves using spin button application of spreadsheet software was used in designing the proposed sampling plans. A few sampling plans (single, double and multiple) with various values of n, c, and other relevant parameters were generated to get the data for AQL and LTPD. The proposed single, double, and multiple sampling plans are presented respectively in Tables 3, 4 and 5. For a single sampling plan, values of AOQL and LTPD with a variation in n and c have been recorded for comparison. As evident in Table 3, both AQL and LTPD decrease as n increases for a particular value of c. If the values of AQL (0.0045) and LTPD (0.0153) as ascertained from current sampling plan are maintained, then a single sampling plan with n = 400 and c = 3 would be good enough. Thus, it is possible to choose a large number of sets for n and c from Table 3 which is to satisfy or even exceed the specified AQL and LTPD to lead to a suitable SSP design.

Table 3: Values of AQL and LTPD for the various Single Sampling Plans

n	c	c = 1	c = 2	c = 3	c = 4	c = 5	c = 6	c = 7	c = 8	c = 9	c = 10
n = 200	AQL	0.0016	0.0040	0.0066	0.0097	0.0130	0.0163	0.0190	0.0230	0.0270	>0.027
	LTPD	0.0190	>0.027	>0.027	>0.027	>0.027	>0.027	>0.027	>0.027	>0.027	>0.027
n = 300	AQL	0.0011	0.0030	0.0045	0.0064	0.0085	0.0100	0.0130	0.0150	0.0180	0.0200
	LTPD	0.0128	0.0170	0.0220	0.0260	0.0270	>0.027	>0.027	>0.027	>0.027	>0.027
n = 400	AQL	0.0008	0.0020	0.0030	0.0047	0.0064	0.0085	0.0100	0.0116	0.0135	0.0150
	LTPD	0.0094	0.0130	0.0016	0.0190	0.0230	0.0260	0.0270	>0.027	>0.027	>0.027
n = 500	AQL	0.0007	0.0016	0.0025	0.0040	0.0052	0.0064	0.0078	0.0090	0.0100	0.0120
	LTPD	0.0075	0.0100	0.0130	0.0150	0.0182	0.0200	0.0230	0.0256	0.0270	>0.027
n = 600	AQL	0.0050	0.0010	0.0020	0.0042	0.0045	0.0054	0.0066	0.0070	0.0090	0.0100
	LTPD	0.0064	0.0087	0.0190	0.0150	0.0153	0.0170	0.0190	0.0210	0.0230	0.0250
n = 700	AQL	0.0004	0.0011	0.0018	0.0029	0.0034	0.0040	0.0056	0.0066	0.0075	0.0087
	LTPD	0.0054	0.0070	0.0094	0.0110	0.0013	0.0140	0.0166	0.0180	0.0200	0.0210
n = 800	AQL	0.0004	0.0010	0.0016	0.0020	0.0030	0.0040	0.0049	0.0056	0.0060	0.0075
	LTPD	0.0047	0.0060	0.0082	0.0090	0.0110	0.0130	0.0140	0.0160	0.0170	0.0180

As shown in Table 4, for double sampling plan (DSP), several combinations with different value of n_1, n_2, Ac_1, Ac_2, Re_1 and Re_2 were simulated to generate the relevant attributes of OC curve. The AQL and LTPD values that were close to that of the current sampling plan (AQL=0.0045 and LTPD = 0.0153) are presented. For instance, sampling plan 5 having n_1 = 300, n_2 = 600, Ac_1 = 1, Re_1 = 3, Ac_2 = 6, and Re_2=7 results in AQL of 0.003 and LTPD of 0.013 which can comfortably replace the current SSP. The plan 6 appears to be even better.

Table 4: Attributes of OC Curve data for proposed Double Sampling Plan (DSP)

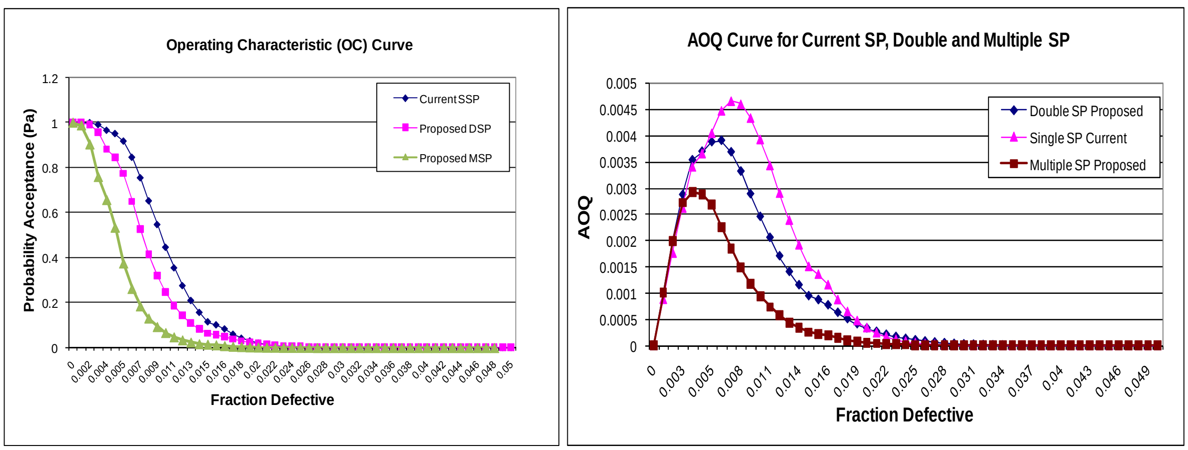
DSP No.	n_1	n_2	Ac_1	Re_1	Ac_2	Re_2	AQL	LTPD	AOQL
Plan 1	400	200	1	3	5	5	0.0025	0.013	0.00376
Plan 2	400	200	1	4	3	5	0.0020	0.014	0.00332
Plan 3	400	200	1	3	2	4	0.0025	0.013	0.00376
Plan 4	400	200	1	3	6	7	0.0030	0.013	0.00376
Plan 5	**300**	**600**	**1**	**3**	**6**	**7**	**0.0030**	**0.013**	**0.00389**
Plan 6	600	300	1	3	6	7	0.0020	0.013	0.00278
Plan 7	200	400	1	4	6	7	0.0030	0.019	0.00497

Out of a number of simulated multiple sampling plans (MSP) three are presented in Table 5. Compared to the attributes set by the current SSP, MSP 1 appears to be superior which can be proposed to replace the current SSP.

Table 5: Several data for proposed Multiple Sampling Plan (MSP)

Plan	n	c	Re	AQL	LTPD
Plan 1	$\boldsymbol{n_1 = 400}$, $\boldsymbol{n_2 = 800}$, $\boldsymbol{n_3 = 1200}$	$\boldsymbol{Ac_1 = 1}$ $\boldsymbol{Ac_2 = 4}$ $\boldsymbol{Ac_3 = 9}$	$\boldsymbol{Re_1 = 4}$ $\boldsymbol{Re_2 = 7}$ $\boldsymbol{Re_3 = 9}$	**0.003**	**0.010**
Plan 2	$n_1 = 200$, $n_2 = 200$, $n_3 = 200$	$Ac_1 = 1$ $Ac_2 = 4$ $Ac_3 = 9$	$Re_1 = 4$ $Re_2 = 7$ $Re_3 = 9$	0.005	0.020
Plan 3	$n_1 = 400$ $n_2 = 400$ $n_3 = 400$	$Ac_1 = 1$ $Ac_2 = 4$ $Ac_3 = 9$	$Re_1 = 4$ $Re_2 = 7$ $Re_3 = 9$	0.003	0.012

The OC curves for the current SSP, proposed DSP (Plan 5) and MSP (Plan 1) are presented in Figure 3. In general, the OC and AOQ functions are known as protection measures given by the sampling plan to the producer as well as the consumer. It is evident that the OC curve for the DSP is superior to that of the SSP whereas the OC curve MSP looks best among the three sampling plans.



(a) (b)

Figure 3: (a) OC Curves (b) AOQ curves for Current SSP, proposed DSP and MSP

AOQ varies with the incoming quality or fraction defective of the lot and follows a non-linear pattern which is calculated by using relevant equations for SSP, DSP and MSP. The maximum level of AOQ known as AOQL for the SSP, as mentioned earlier, is 0.00464. Using the simulation on AOQ curve for every potential sampling plan, AOQL values were determined. The AOQL for DSP and MSP are found to be 0.0039 and 0.0029 respectively. The lower the value of AOQL, the better is the plan in terms of outgoing quality of the lot reaching the customer. In this context the MSP with the lowest AOQL can be considered to be the best option among the three plans.

Other characteristics of sampling plans such as the average sampling number (ASN) and average total inspection (ATI) are presented in Figure 4. The ASN and ATI are important in the context of costs involved in inspection – usually the lower the values of ASN and ATI, the better are the plans. For an SSP, each and every lot has a sample size of n taken and inspected. So the value of ASN for a single sampling plan is n. But for DSP, the amount of samples inspected varies depending on the design of the plan and the quality of the incoming lot, p. For any given double, multiple or sequential plan, ASN can be calculated assuming all lots come in with a defect level of p. A plot of the ASN, versus the incoming defect level p, describes the sampling efficiency of a given plan. Equation 4 as given below is used for calculation of ASN value for a DSP:

$$ASN = n_1 P_1 + (n_1 + n_2)(1 - P_1) = n_1 + n_2 (1 - P_1) \qquad (4)$$

where P_1 is the probability of a decision on the first sample.

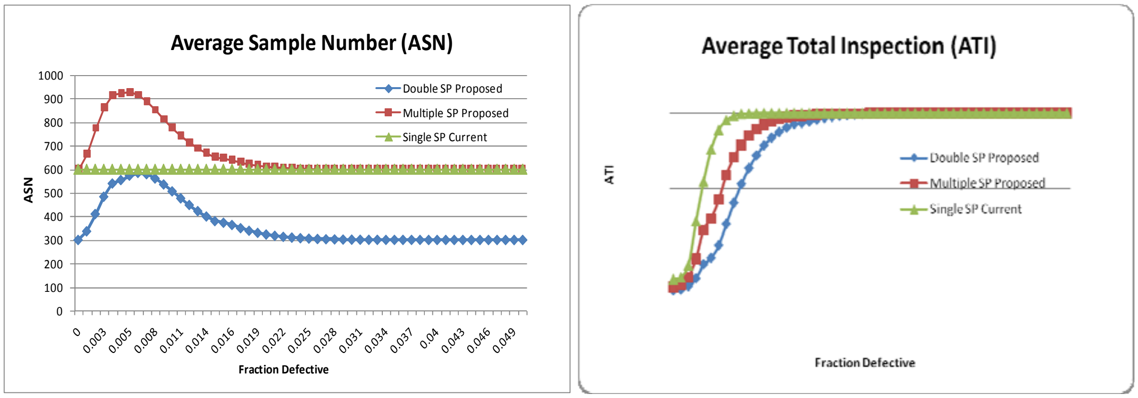
Equation 5 is a generalized form used for ASN calculation for a multiple sampling plan having jth stage,

$$ASN = \sum_{j=1}^{k} \sum_{m=1}^{j} n_m T_j \tag{5}$$

where T_j is probability of termination at the jth stage. For the proposed multiple sampling plan, the value of ASN can be determined by the equation 6:

$$ASN = n_1T_1 + (n_1 + n_2)\ T_2 + (n_1+n_2+n_3)\ T_3 \tag{6}$$

ASN for the current SSP and proposed DSP and MSP are plotted in Figure 4(a). It is apparent that the average sampling number to be conducted by the proposed MSP is on the higher side. But since the inspection conducted at VMI is only visual in nature, higher ASN due to the implementation of MSP is not expected to incur any extra cost.



(a) (b)

Figure 4: (a) ASN Curves and (b) ATI Curves for Current SSP and proposed DSP and MSP

Average Total Inspection (ATI) is defined as the average or expected number of units to be inspected for a lot. ATI is also a function of fraction defective, *p* of the incoming lot. For an SSP, ATI can be calculated by equation 7.

$$ATI = n + (1 - P_a)(N - n) \tag{7}$$

The probability of acceptance of a lot on the basis of inspected outcome on the collected sample of size, *n* without further rectification or 100% inspection of the rest of the lot is P_a. So $(1 - P_a)$ is the probability of rejection or non-acceptance of the lot on the basis of the sample and the rest of the lot i.e. (N –n) items are to be inspected. By applying similar approach, ATI for DSP and MSP has been evaluated as function of fraction defective, p or incoming lot quality. Figure 4(b) shows ATI curves for SSP, DSP and MSP.

4.0 Comparative evaluation of performance

The salient features of the SSP, DSP and MSP as found from the simulation are summarized in Table 5.

Table 5: Summary of the Current SSP and proposed DSP and MSP

Type of Sampling Plan / Characteristics of the plan	Current SSP	DSP (Plan 8)	MSP (Plan 1)
Sample Size, n	n = 600	n_1= 300, n_2= 600	n_1 = 400, n_2 = 800, n_3 = 1200
Acceptance Number, *Ac*	c = 5	Ac_1=1, Ac_2=3	Ac_1 =1, Ac_2=4, Ac_3=9,
Rejection Number, *Re*	Not applicable	Re_1=6, Re_2 =7	Re_1=4, Re_2=7, Re_3=9
Acceptable Quality Level (AQL)	0.00450	0.0030	0.0030
Lot Tolerance Percent Defective (LTPD)	0.01530	0.0130	0.0100
Average Outgoing Quality Limit (AOQL)	0.00464	0.0038	0.0029

Though there are slight increases in the ASN and ATI values, the basic criteria of the proposed sampling plans (DSP and MSP) such as AQL, LTPD and AOQL exhibit superior positions compared those rendered by the current SSP with rectification. Since attributes look best, MSP may be proposed for implementation. An observation on the current sampling plan reveals that an operator normally takes about 2-3 minutes for the visual inspection of 200 IC units contained in four magazines. Thus the inspection time of the sample of size 600 ICs (200 taken three times) as required by an operator should not exceed more than nine minutes. But the total production time for a lot of 5000 units is about 45 minutes. So the operator's 36 minutes spare time can be utilized by introducing the proposed multiple sampling plan having a larger sample size.

The number of IC units required to be inspected as samples in MSP can be 400, 1200 (i.e. 400+800), or 2400 (i.e. 400+800+1200). If, out of 400 (n_1) ICs taken as first sample, the number of defectives ≤ 1, no further inspection is necessary and the whole lot is to be accepted. But if number of defectives > 4 in the first sample, the lot is to be rejected and the remaining 4600 ICs are needed to be inspected. But out of 4,600 units 2,400 can be checked by the operator in parallel with continuation of production. So the remaining 2,200 should be treated as WIP for which additional human resources are needed. Similarly, the probable influences of acceptance or rejection based on the second and third samples on the WIP are summarized in Table 6.

Table 6: Current SSP and proposed MSP: Possible Impact on WIP

Sampling Plan	Sampling Plan Parameters	Possible maximum WIP level at VMI	Reduction of WIP
SSP (Current)	n = 600, c = 5	5000 - 600 = 4400 ICs	0
MSP (Proposed)	n_1 = 400, $Ac_1 = 1$, $Re_1 = 4$	5000 – 400 - 2400 = 2200 ICs	50.00%
	n_2 = 800, $Ac_2 = 4$, $Re_2 = 7$	5000 -1200 – 1400 = 2400 ICs	45.45%
	n_3 = 1200, $Ac_3 = 9$, $Re_3 = 9$	5000 - (400+800+1200) = 2600 ICs	40.90%

As depicted in Figure 5, the operator's inspection time (as shown by the shaded boxes) can be better planned and utilized with the proposed sampling plan.

Current SSP: Inspection time (9 minutes) when defectives > 5 in 600; WIP = 4,400 ICs

3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min

Proposed MSP: Inspection time (42 minutes) when defectives > 4 in 400; WIP = 2,200 ICs

3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min

Proposed MSP: Inspection time (39 minutes) when defectives > 7 in 400 + 800; WIP = 2,400 ICs

3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min

Proposed MSP: Inspection time (36 minutes) when defectives > 9 in 400+800+1200; WIP = 2,600 ICs

3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min	3min

Figure 5: Operator's inspection workload and WIP for VMI with current SSP and proposed MSP

Implementation of the proposed plan for VMI is to lower the level of possible WIP inventory, though the burden on operator would increase by remaining occupied with inspection during the production time of a lot. The contribution of the new plan is the reduction of the maximum number of IC units to be inspected in case a lot is required to undergo 100% inspection. Under the current practice with SSP, the number of remaining IC units to be rectified with 100% inspection following rejection is 4,400 whereas this value would be reduced to a maximum of 2,600 with the proposed MSP. Thus there is a scope of substantial reduction in WIP inspection. Upon implementation of this plan the probable maximum level of WIP, occurring in case of the need for 100% inspection, is reduced by about 40% leading to a shorter cycle time for lot inspection.

5.0 Conclusions

Incorporation of the proposed multiple sampling plan for VMI instead of the current SSP is deemed to have some positive impacts in streamlining the workload including reduction of level in possible WIP and shorter production cycle time. Though the operator would be more engaged in inspection activities during the production time of a lot, the benefits are considerable. The contribution of the new plan to be noted is the ease in the production system from its current state of turbulence. Anxiety and nervousness of the operator and the supervisor engaged with the sampling for VMI can also be minimized through substantial reduction of the possible maximum level of the remaining units to be inspected for a lot. With the introduction of the proposed multiple sampling plan, the inspection work for the WIP resulting from 100% inspection would be possible to be completed in a shorter time. Moreover, by engaging an additional operator from another line or workstation, or by allocating the responsibility to an operator who is occupied with flexible duty, the process can be much smoother with a stable production system.

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